

FIG. 1C

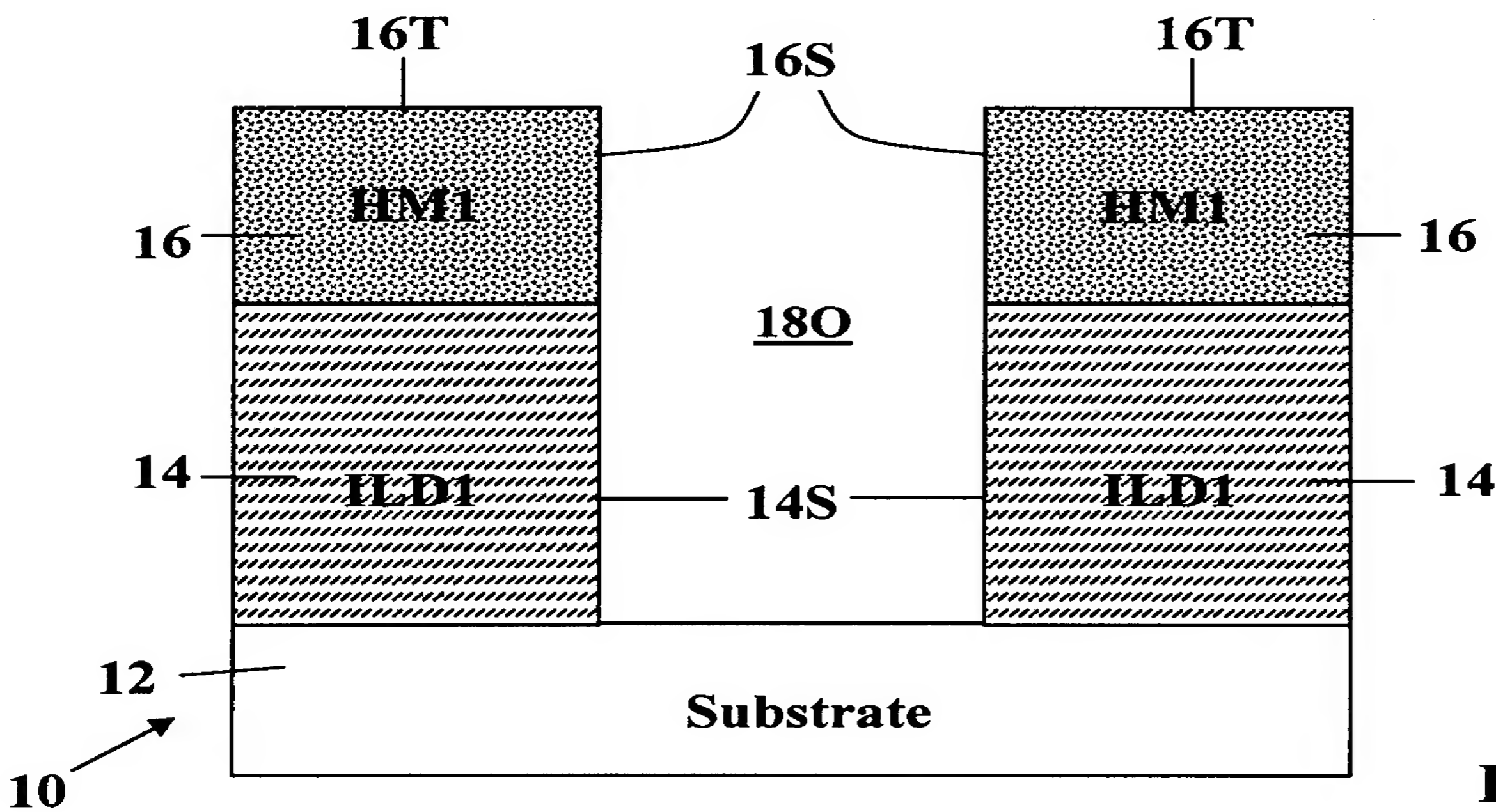
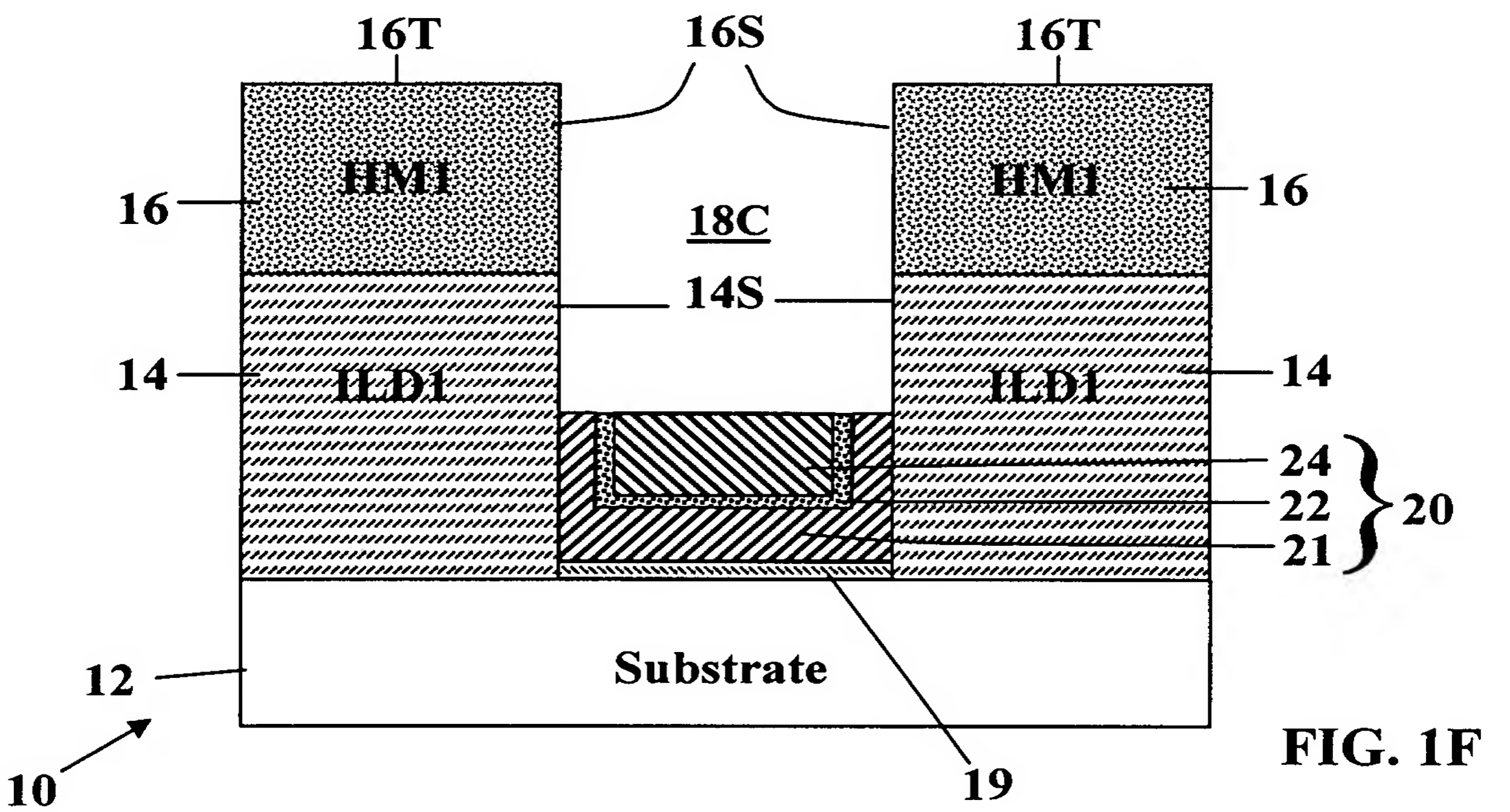
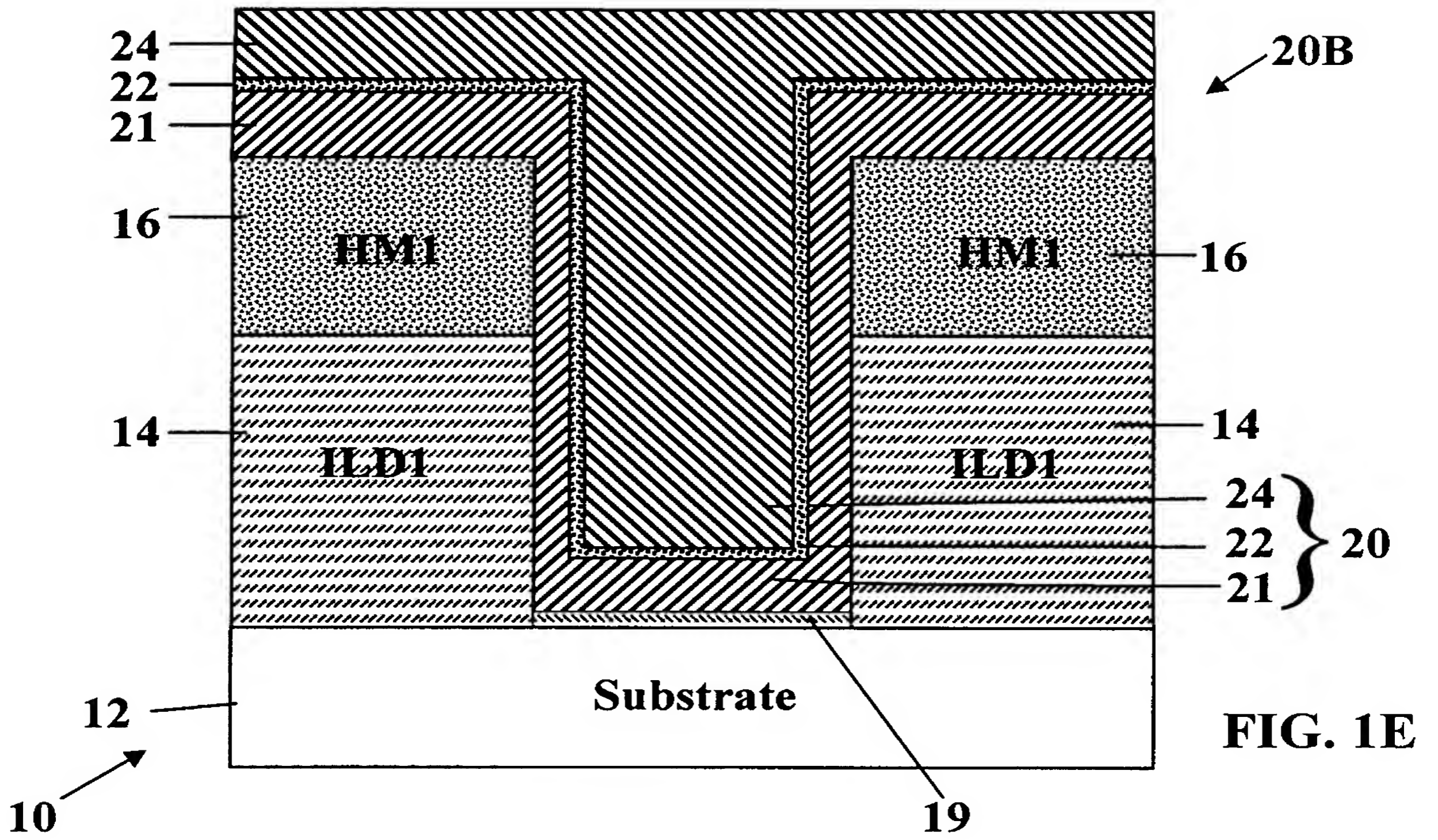
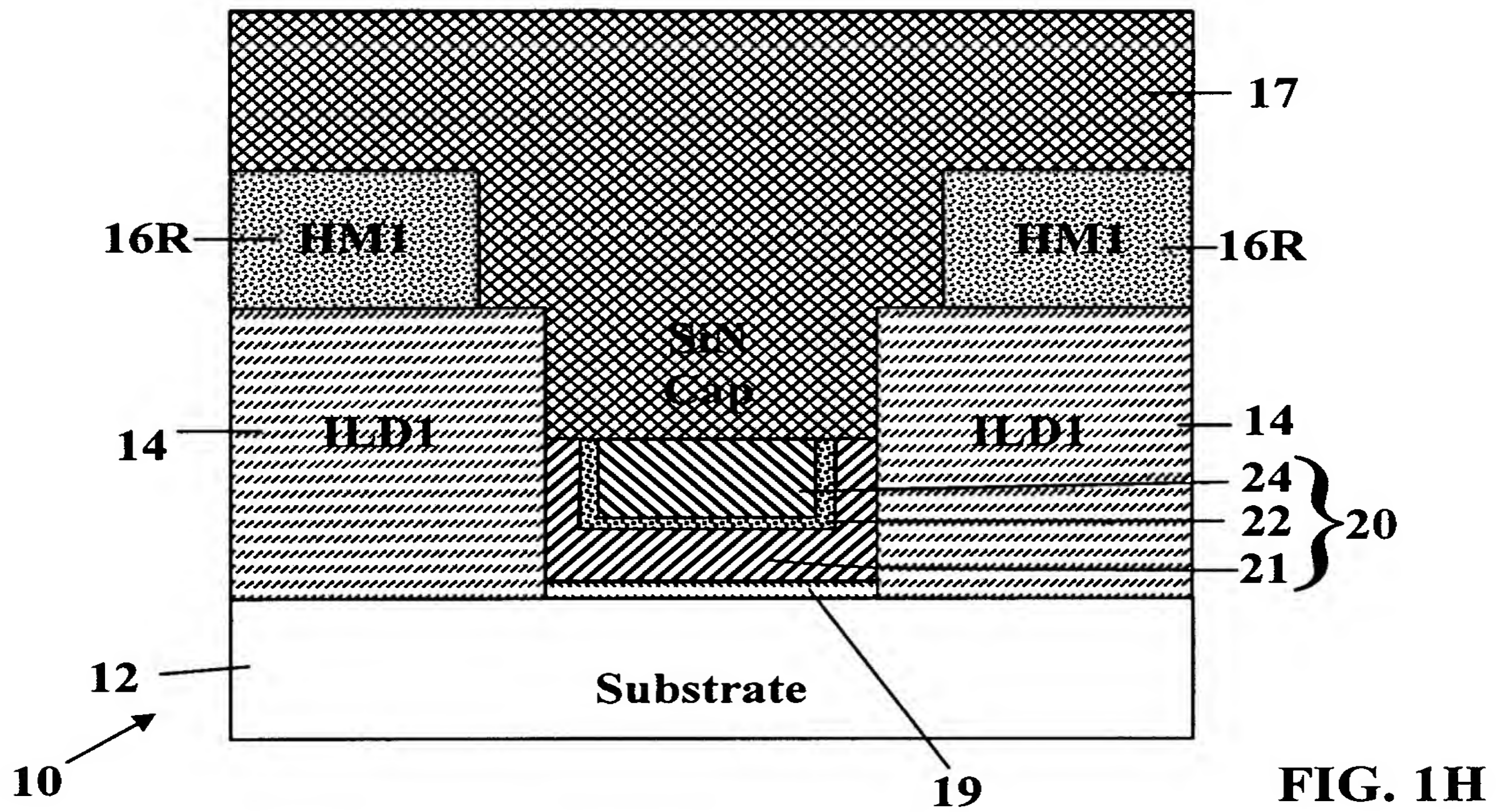
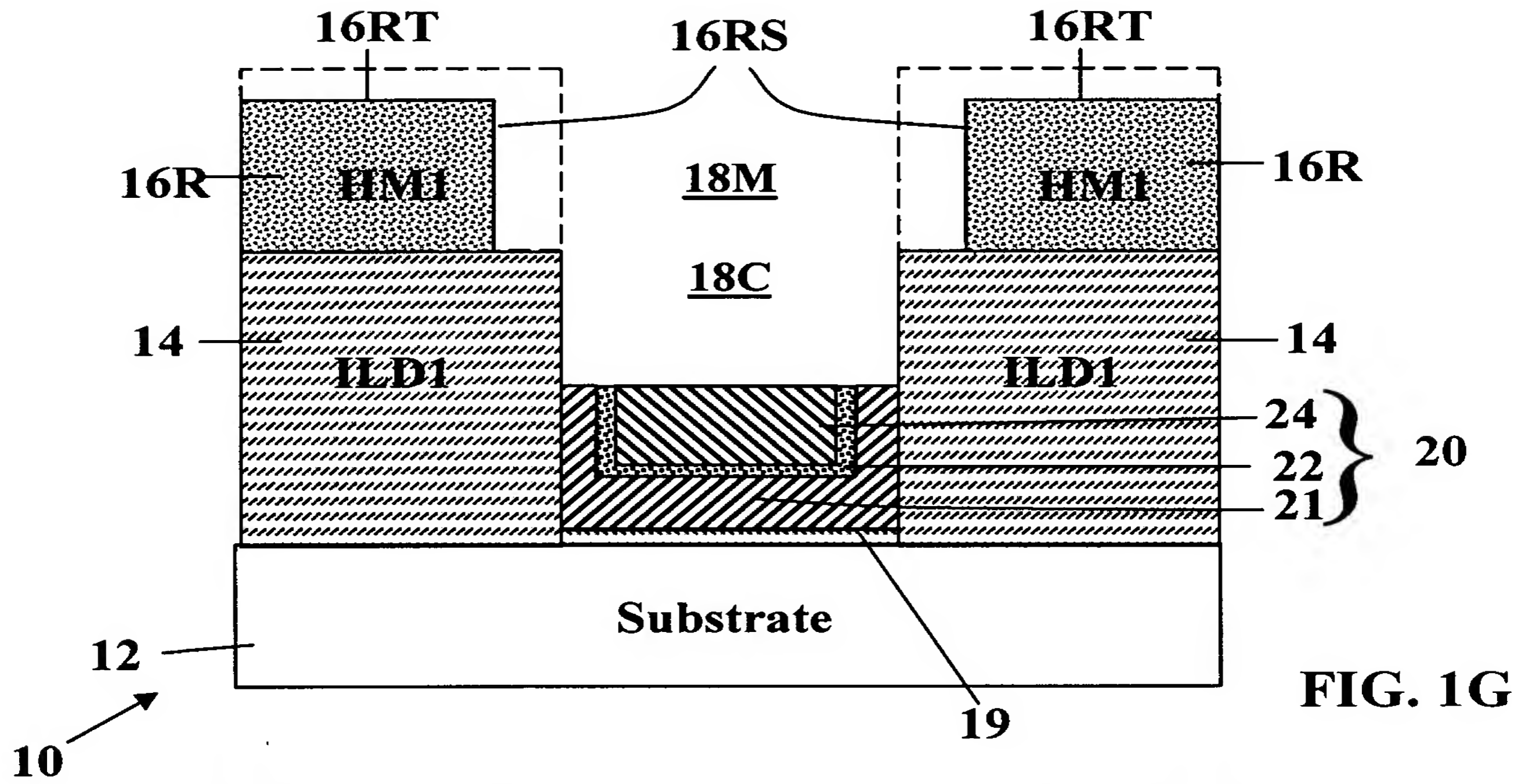


FIG. 1D





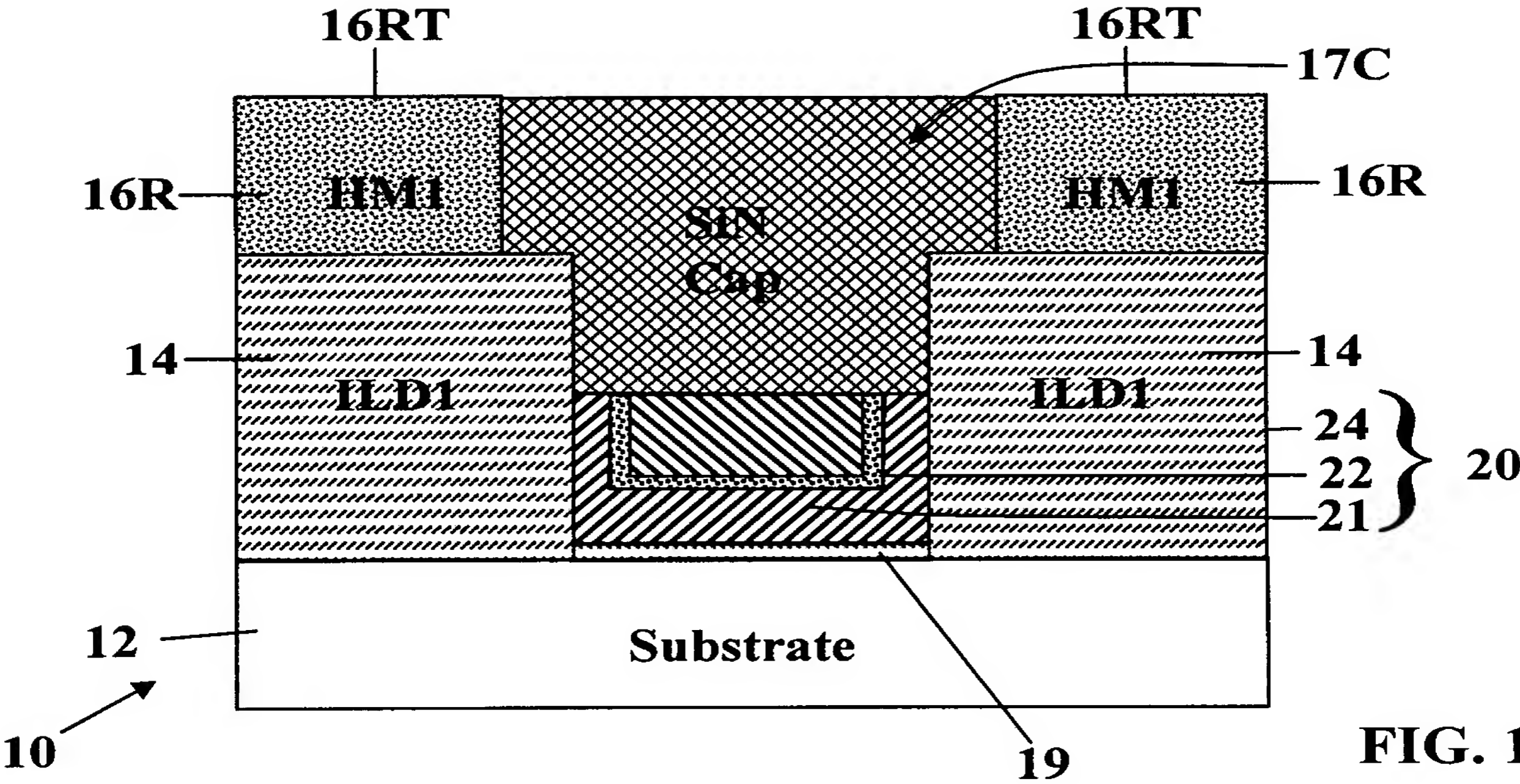


FIG. 1I

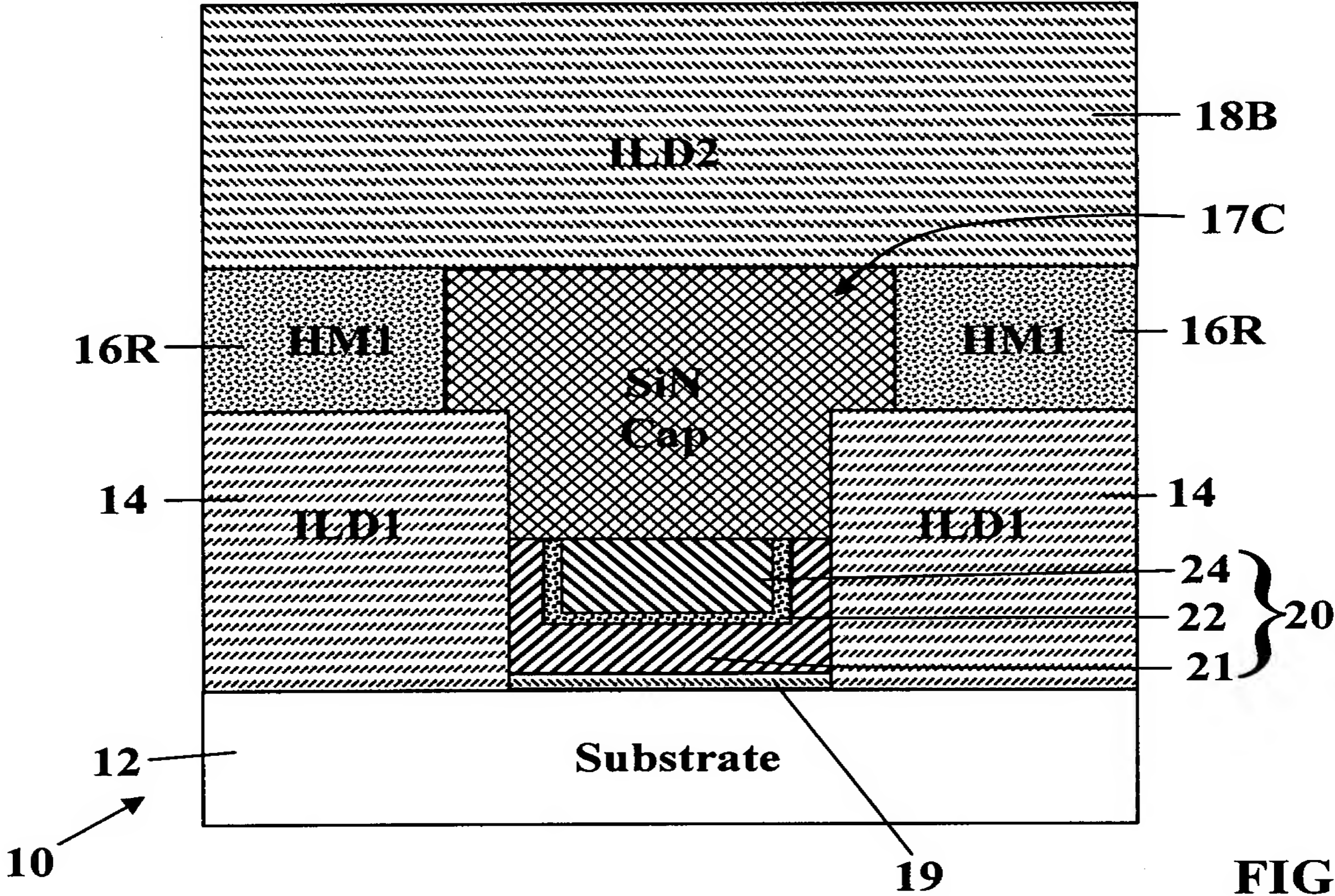


FIG. 1J

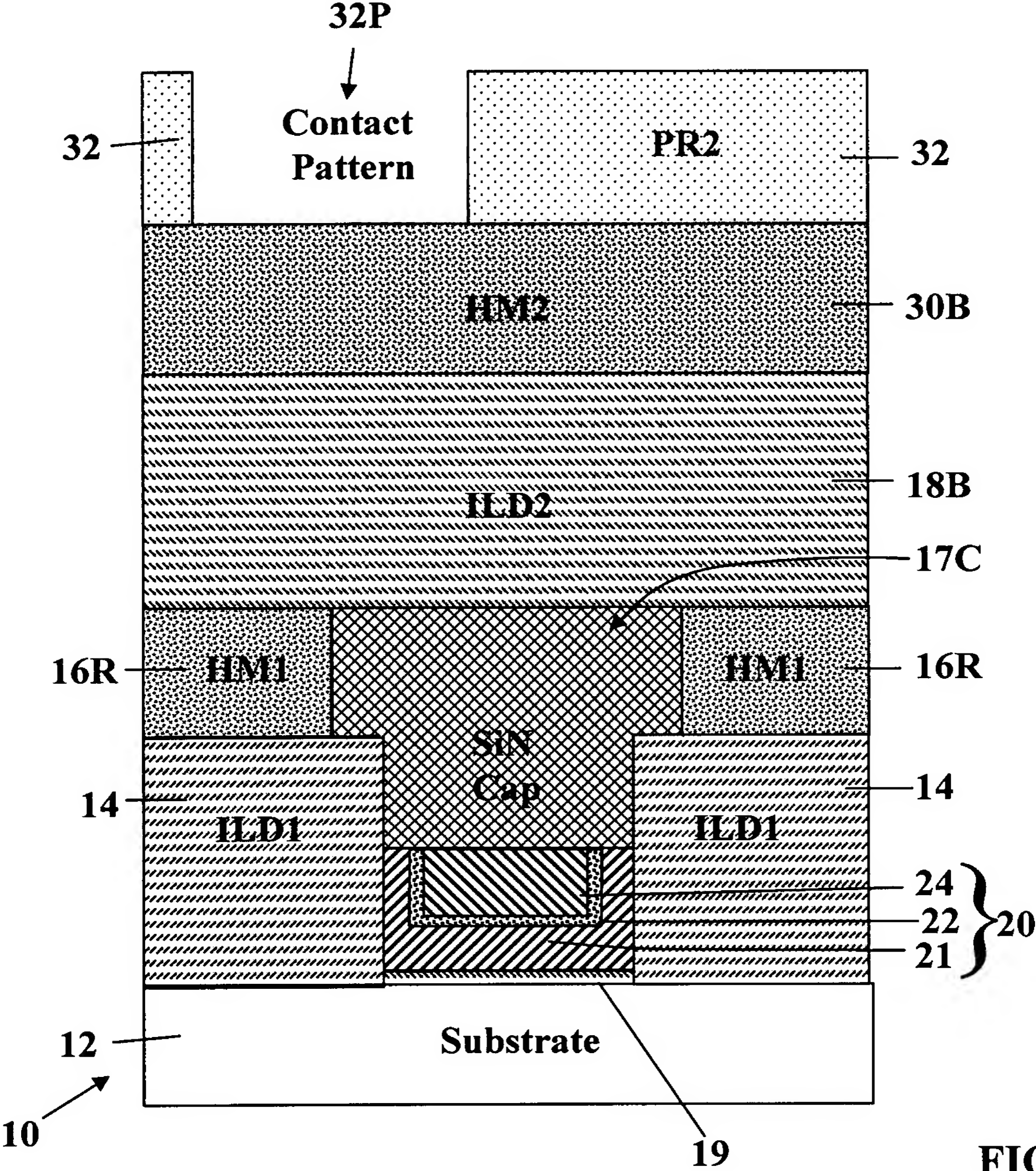


FIG. 1K

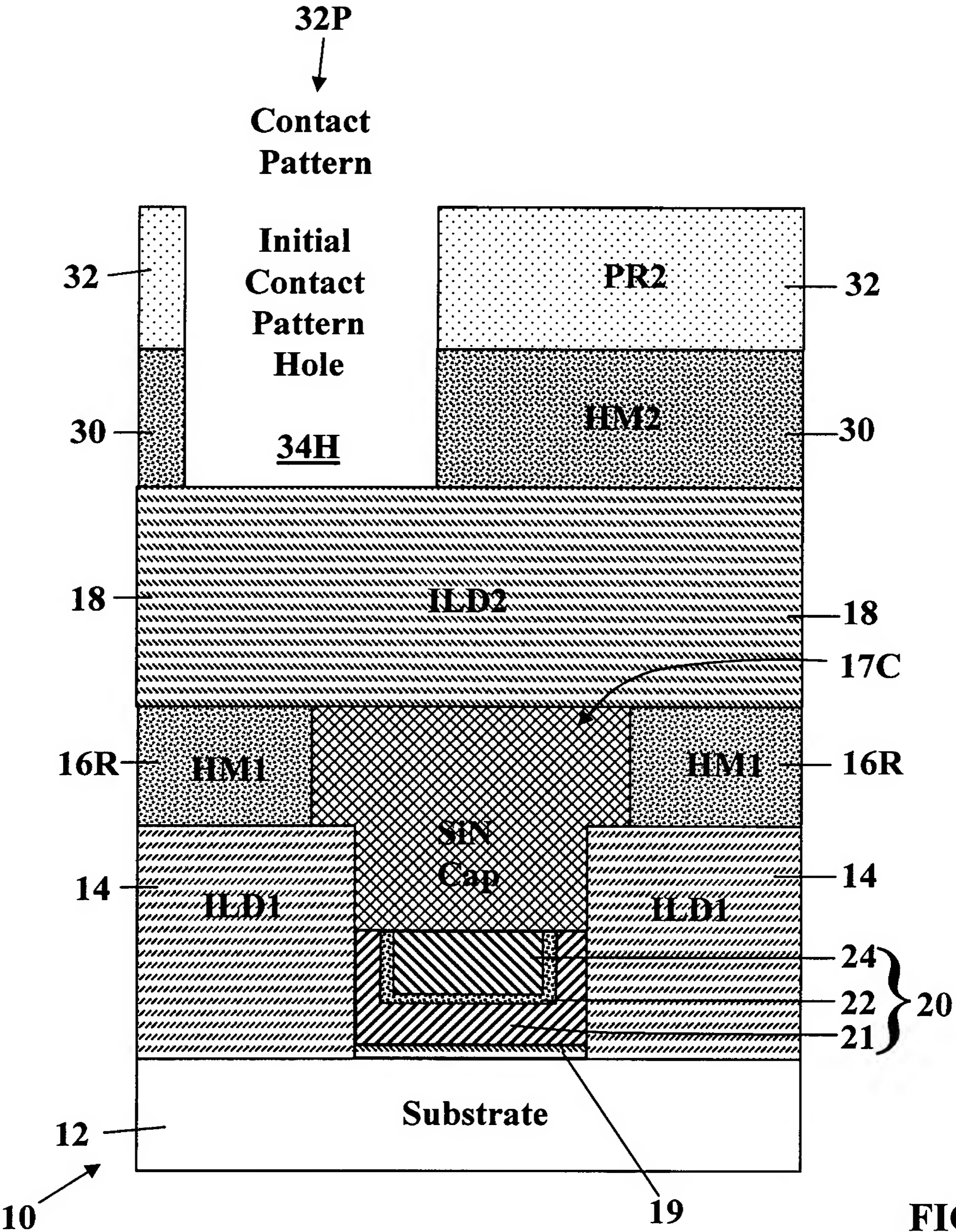


FIG. 1L

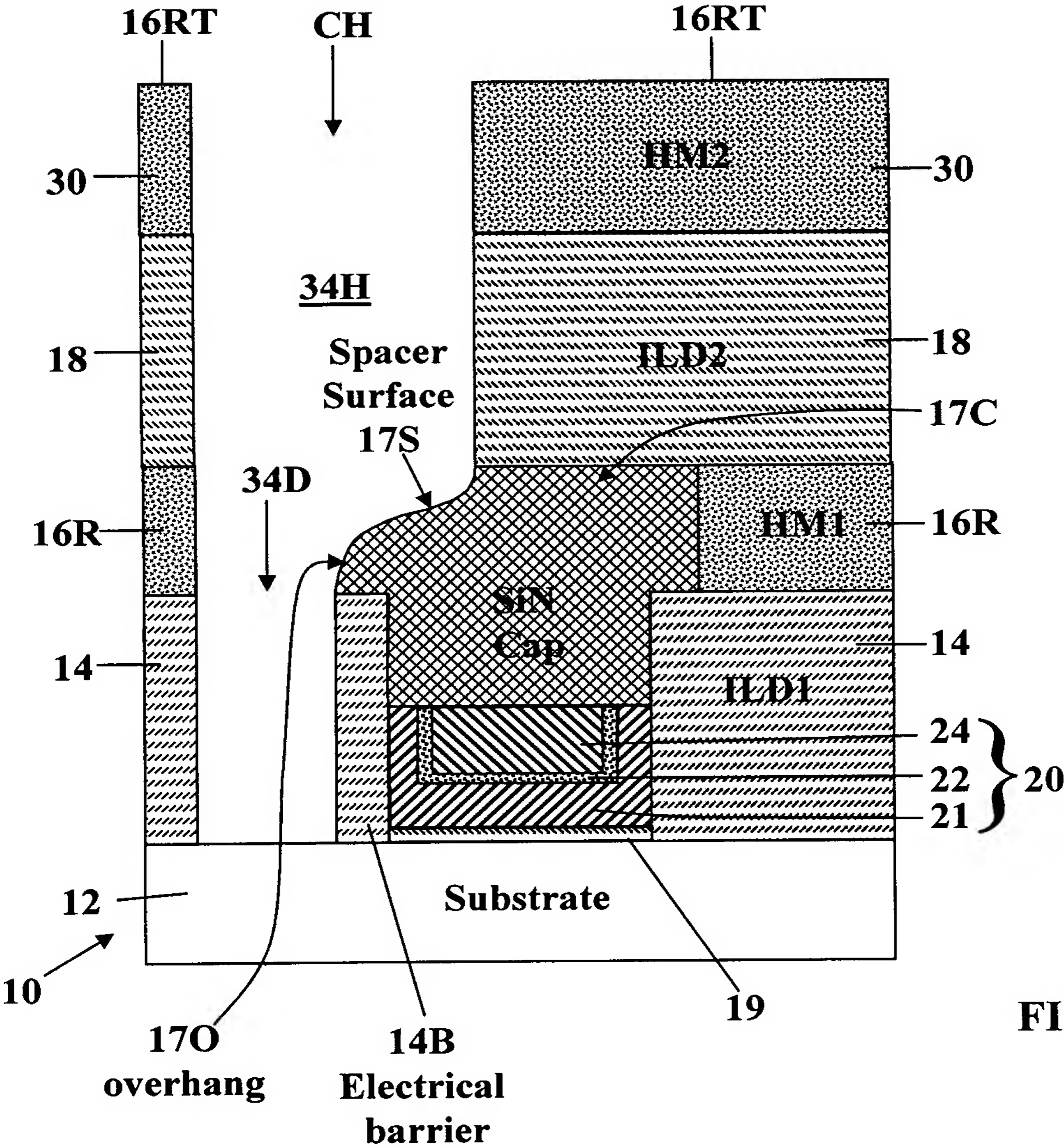
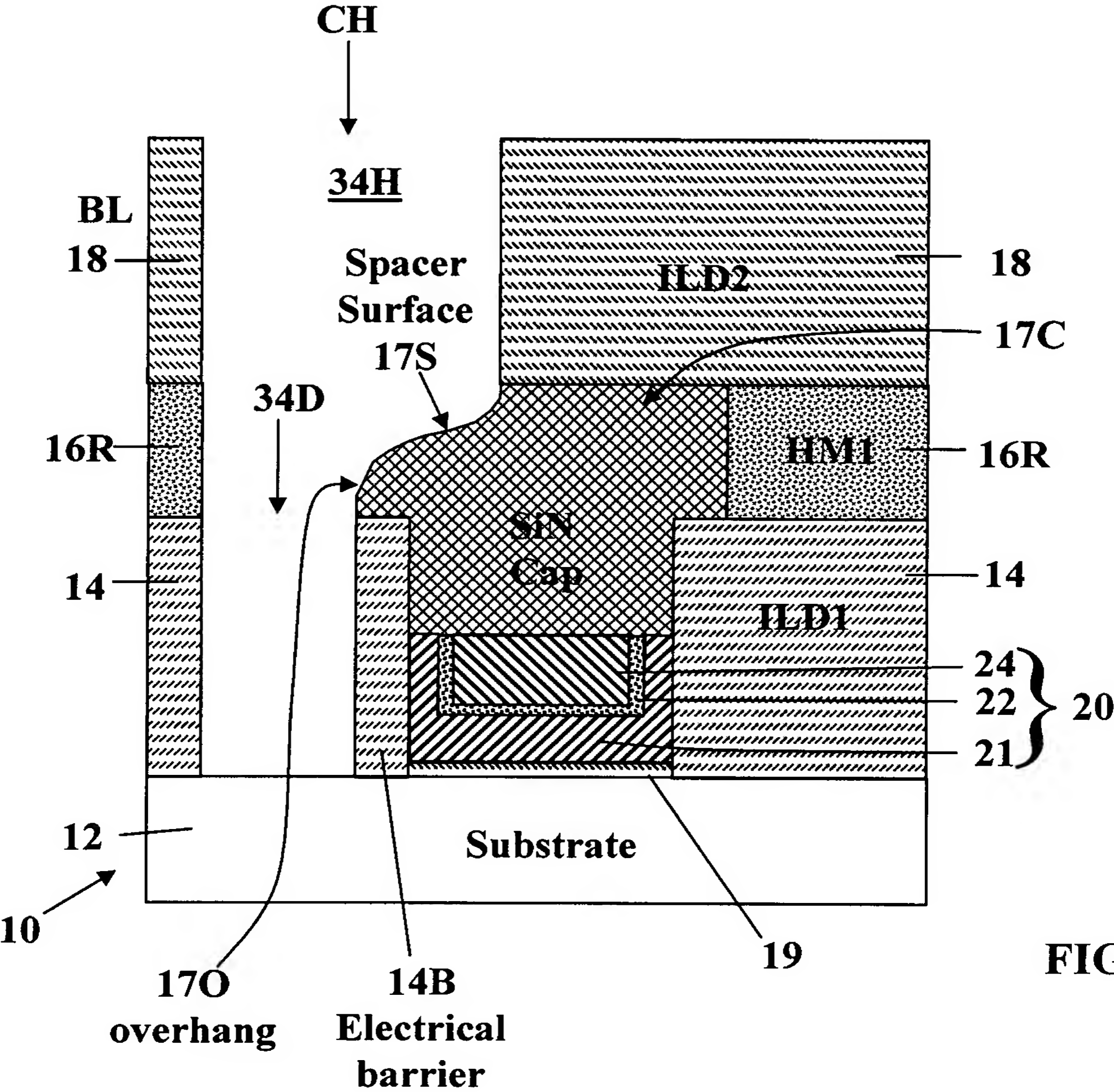


FIG. 1M



10/26

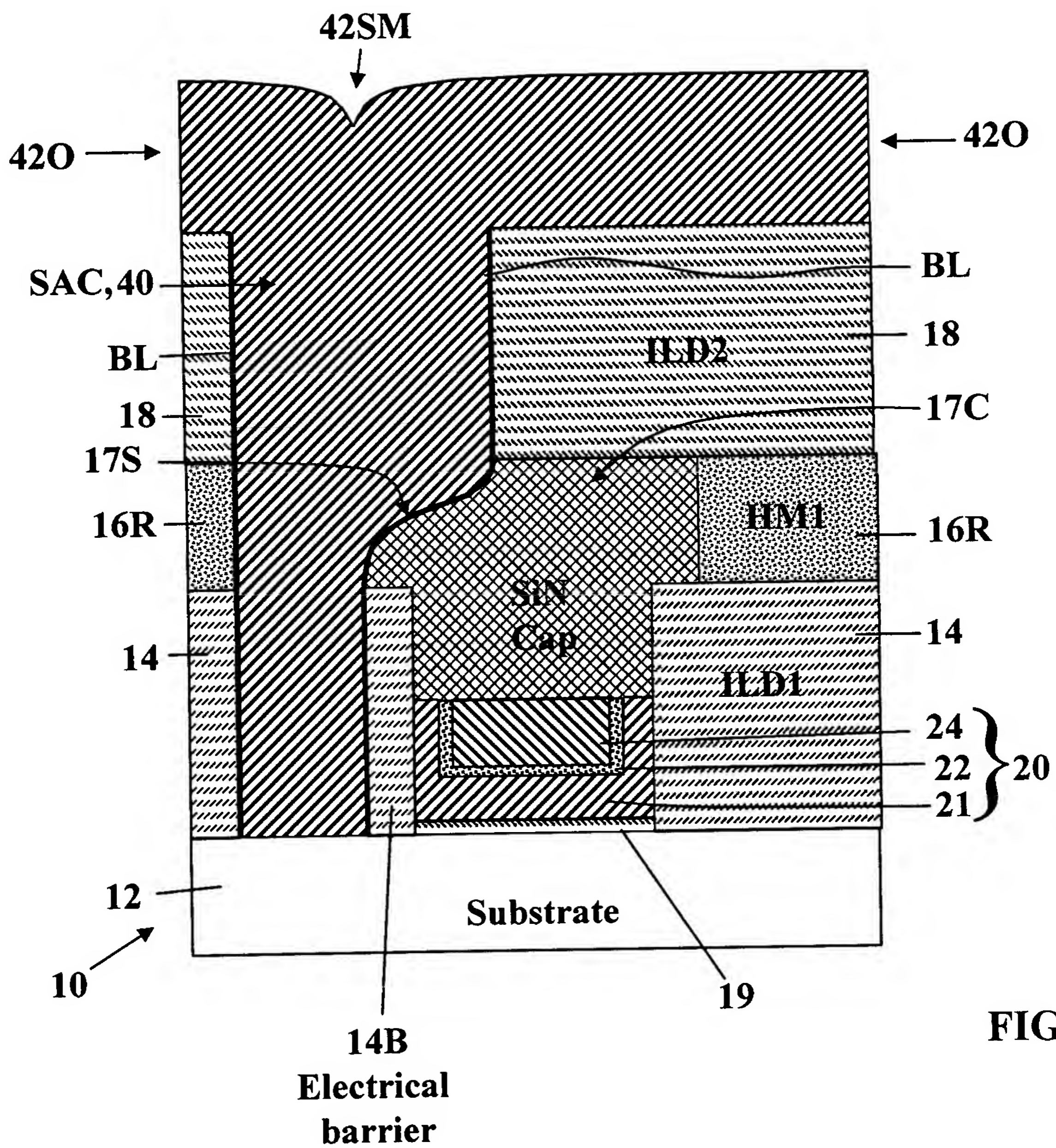


FIG. 10

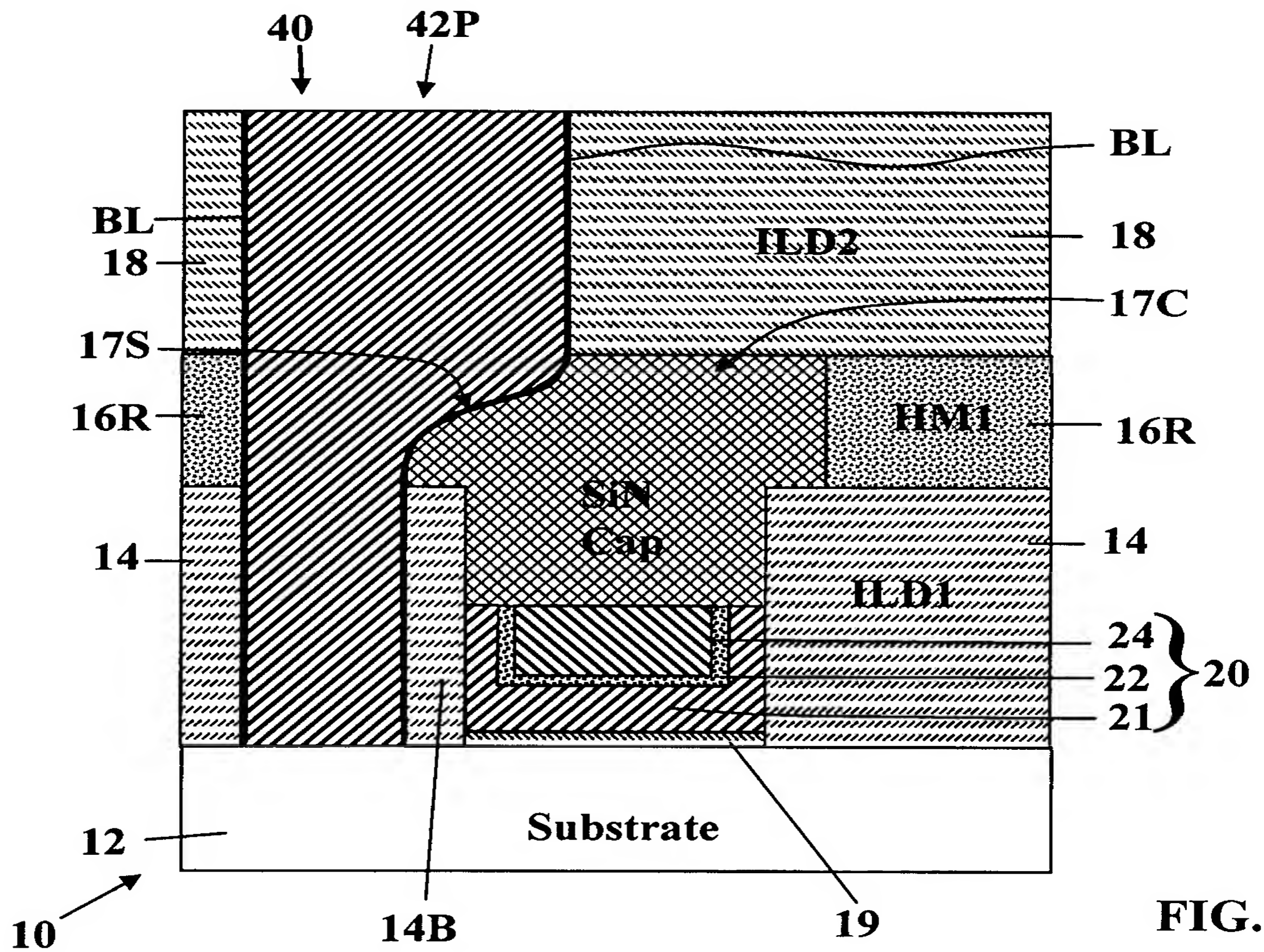


FIG. 1P

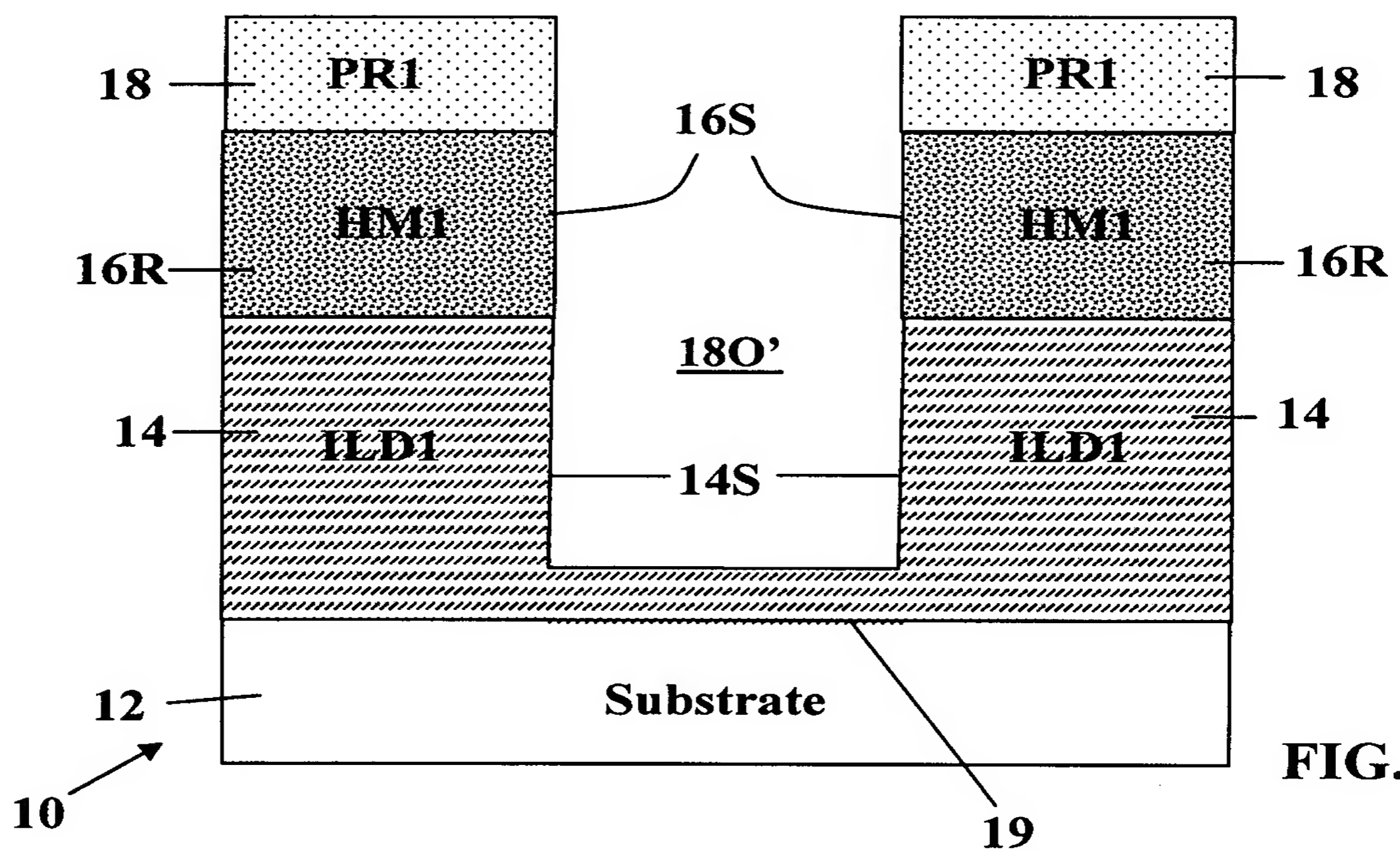


FIG. 1C'

12/26

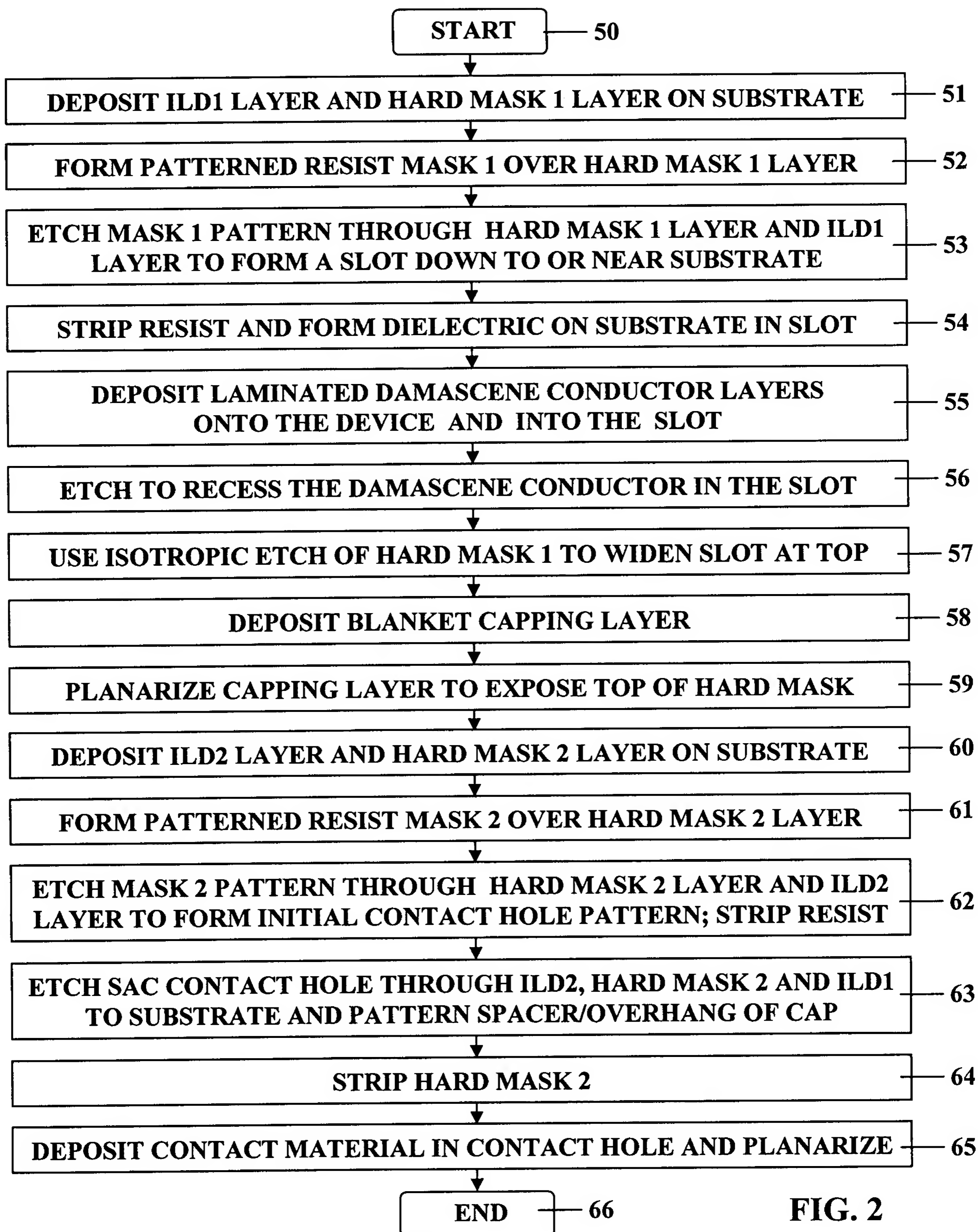
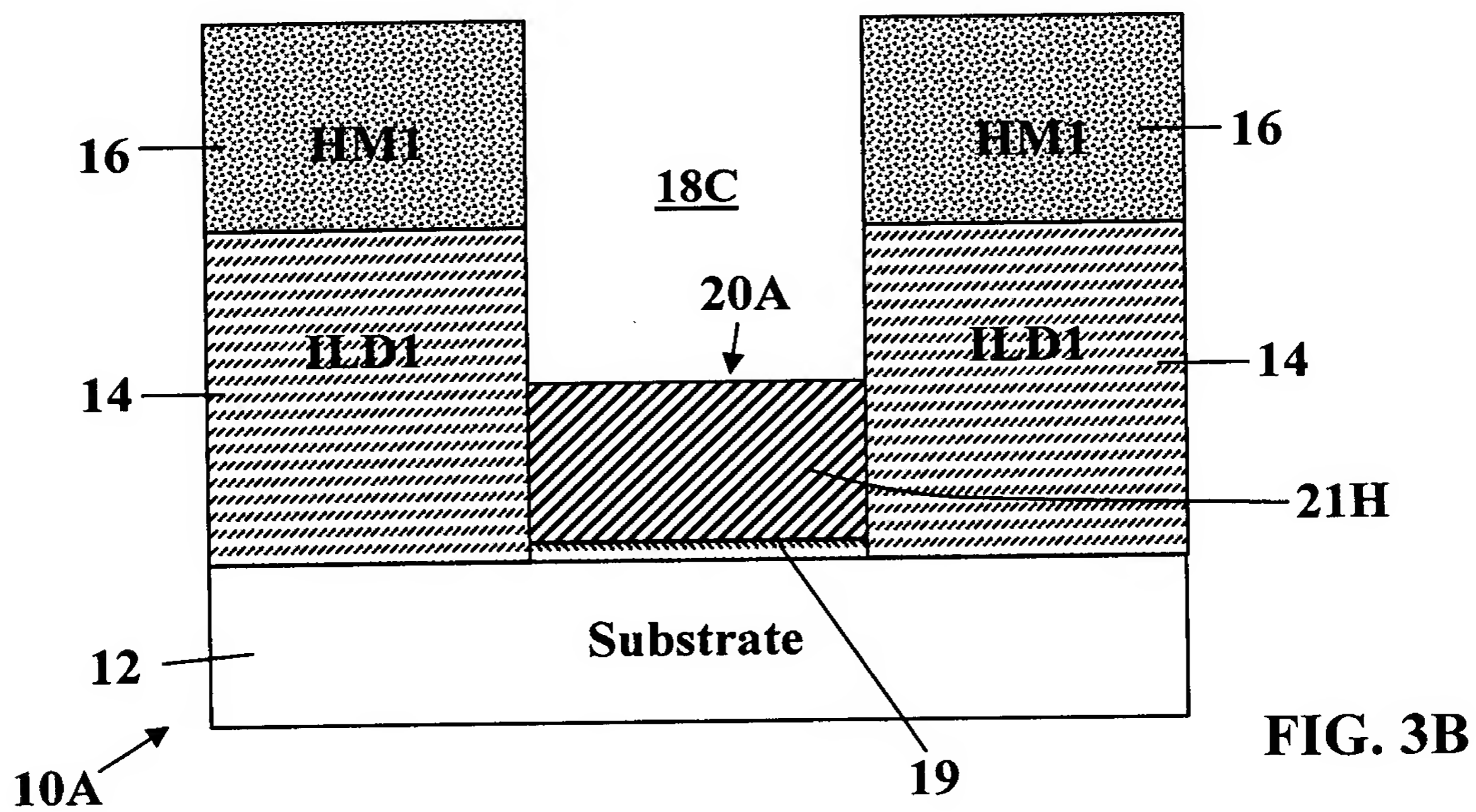
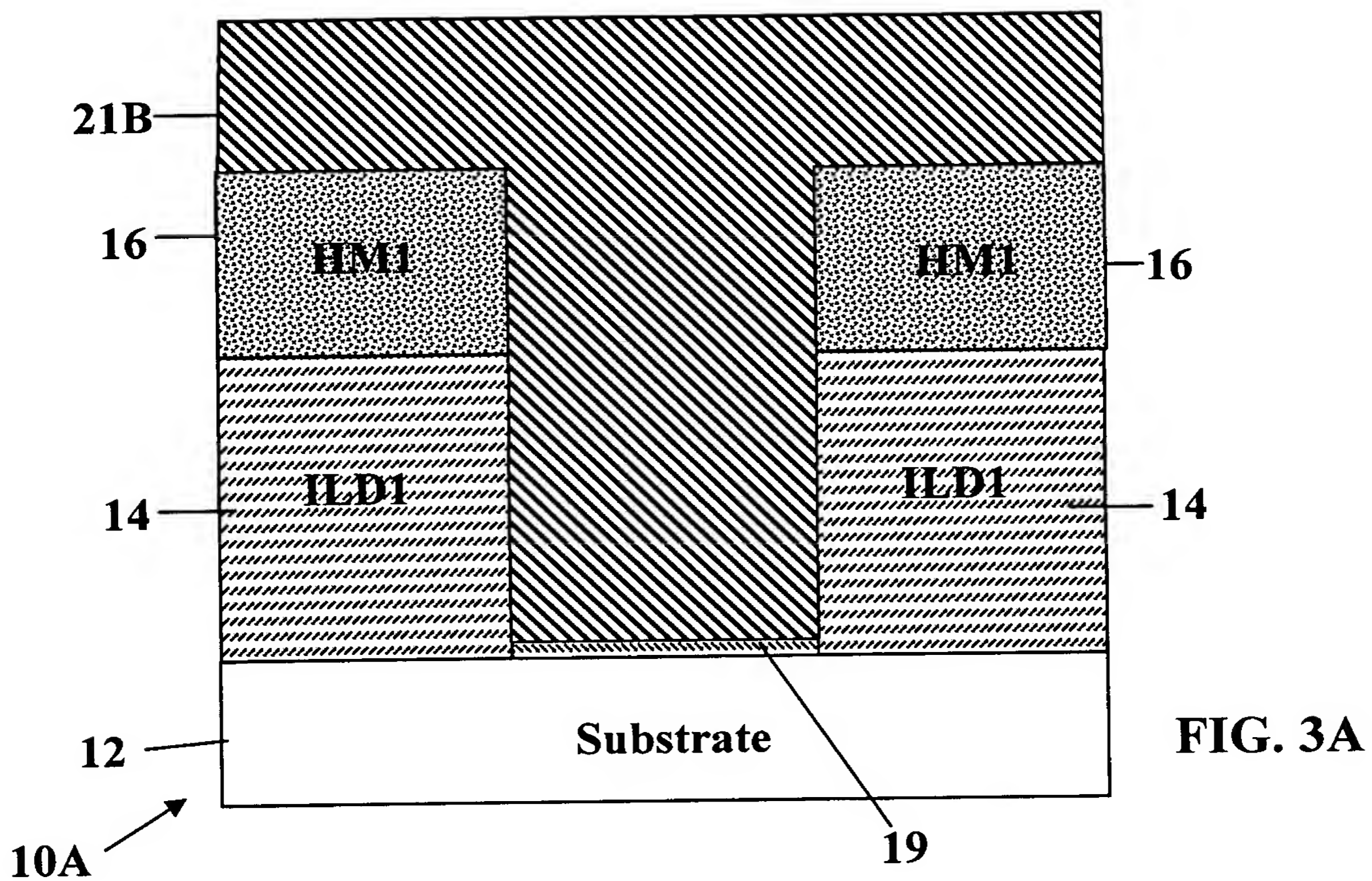
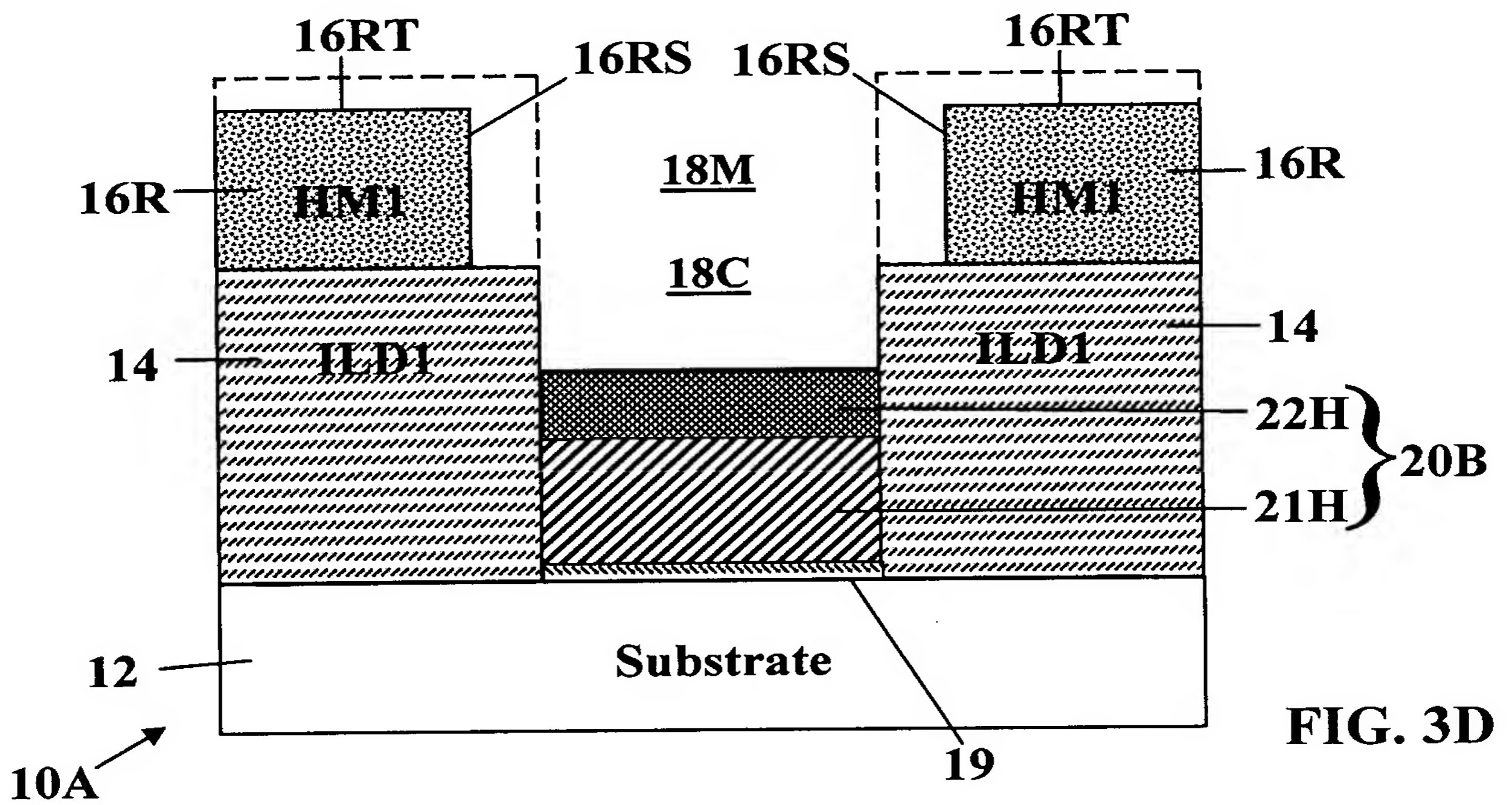
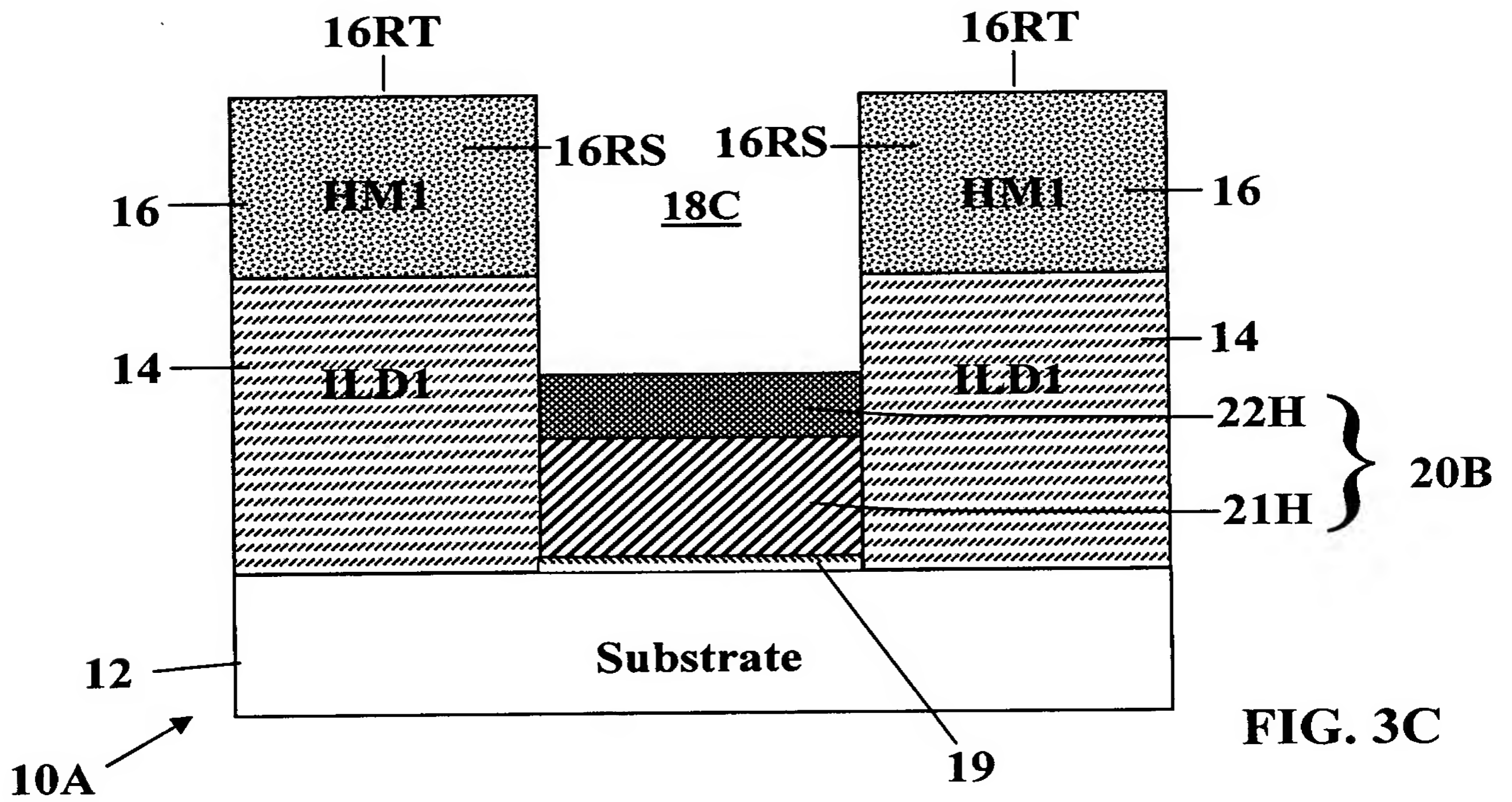
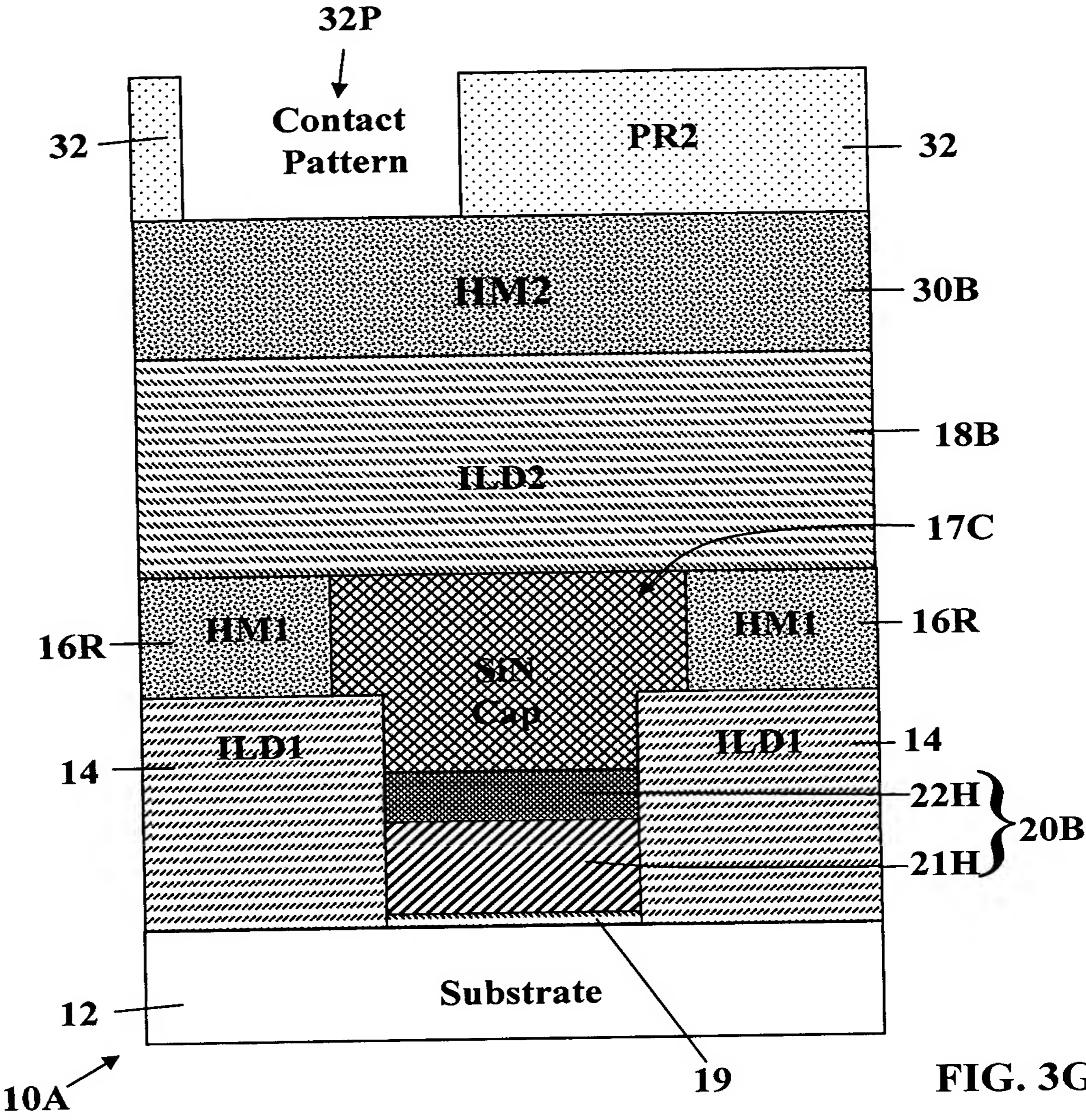


FIG. 2

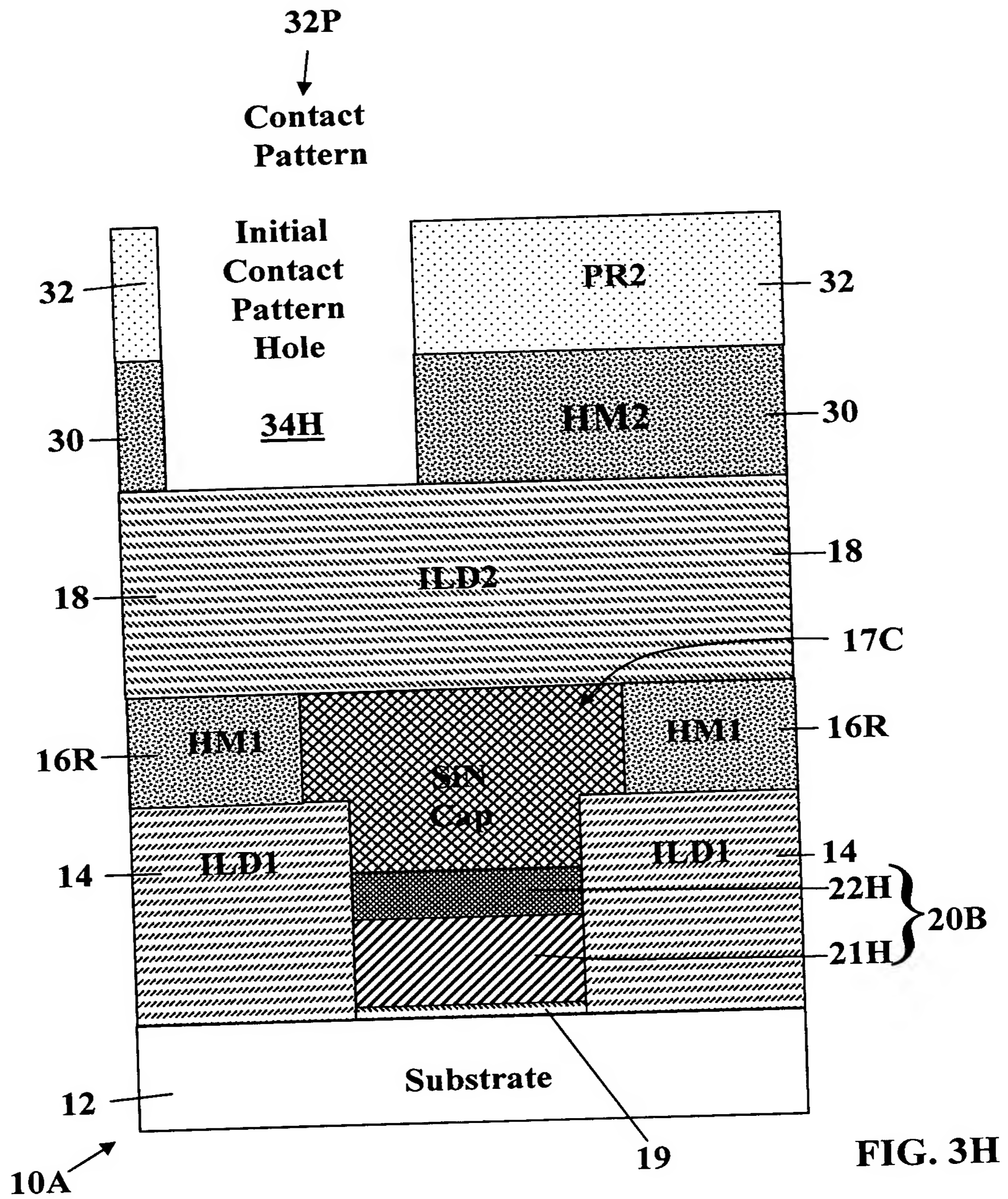




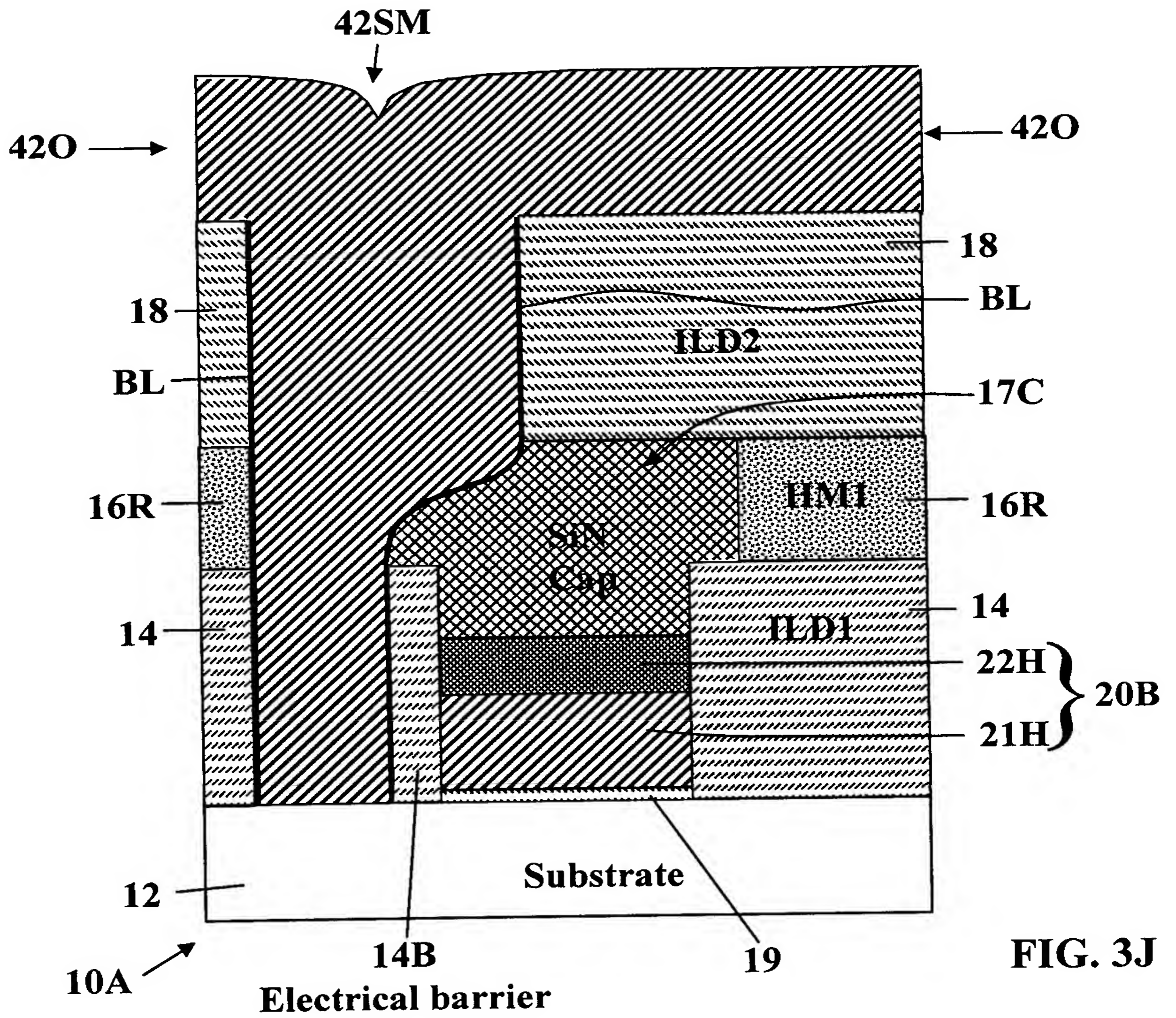


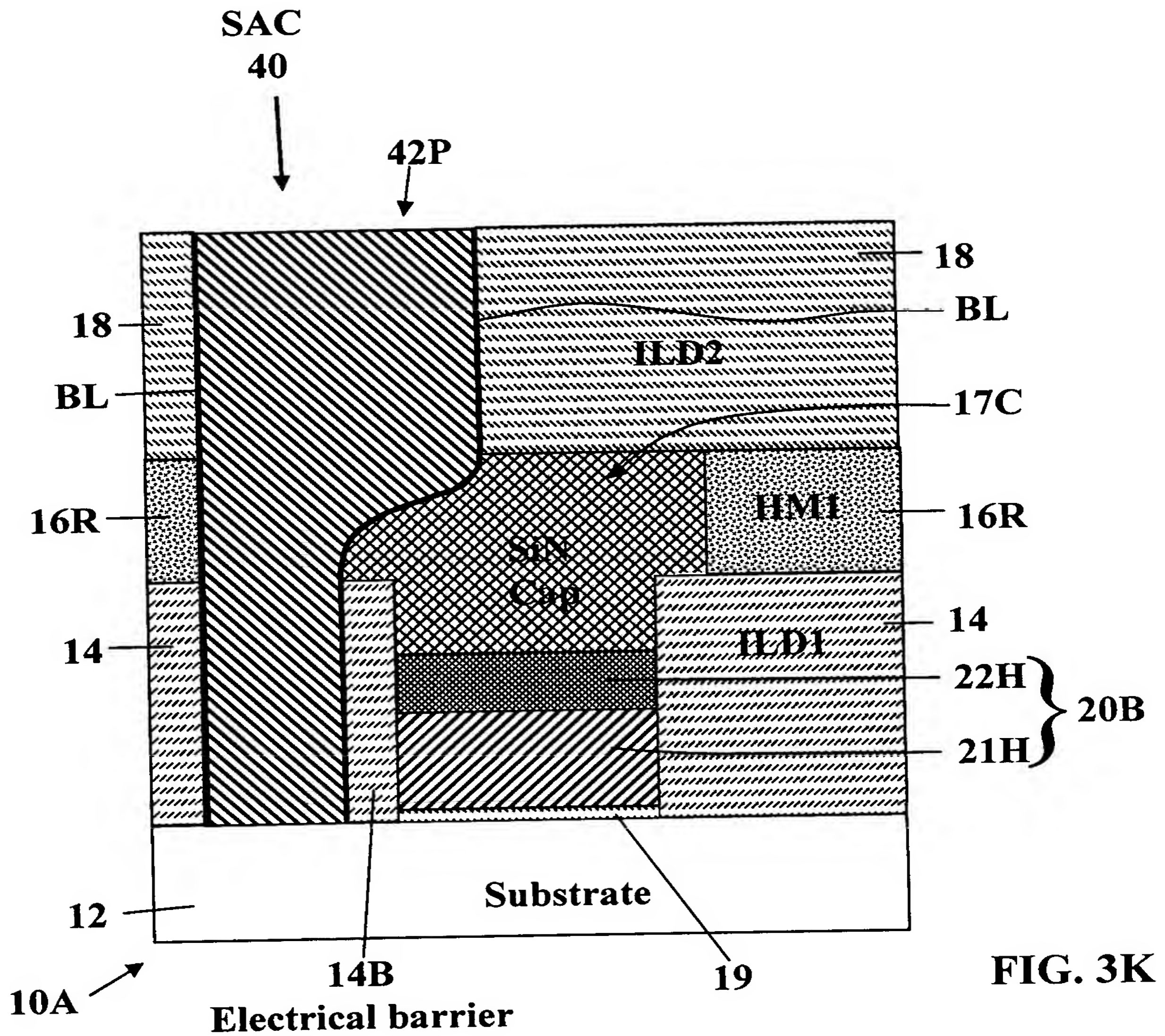


17/26









21/26

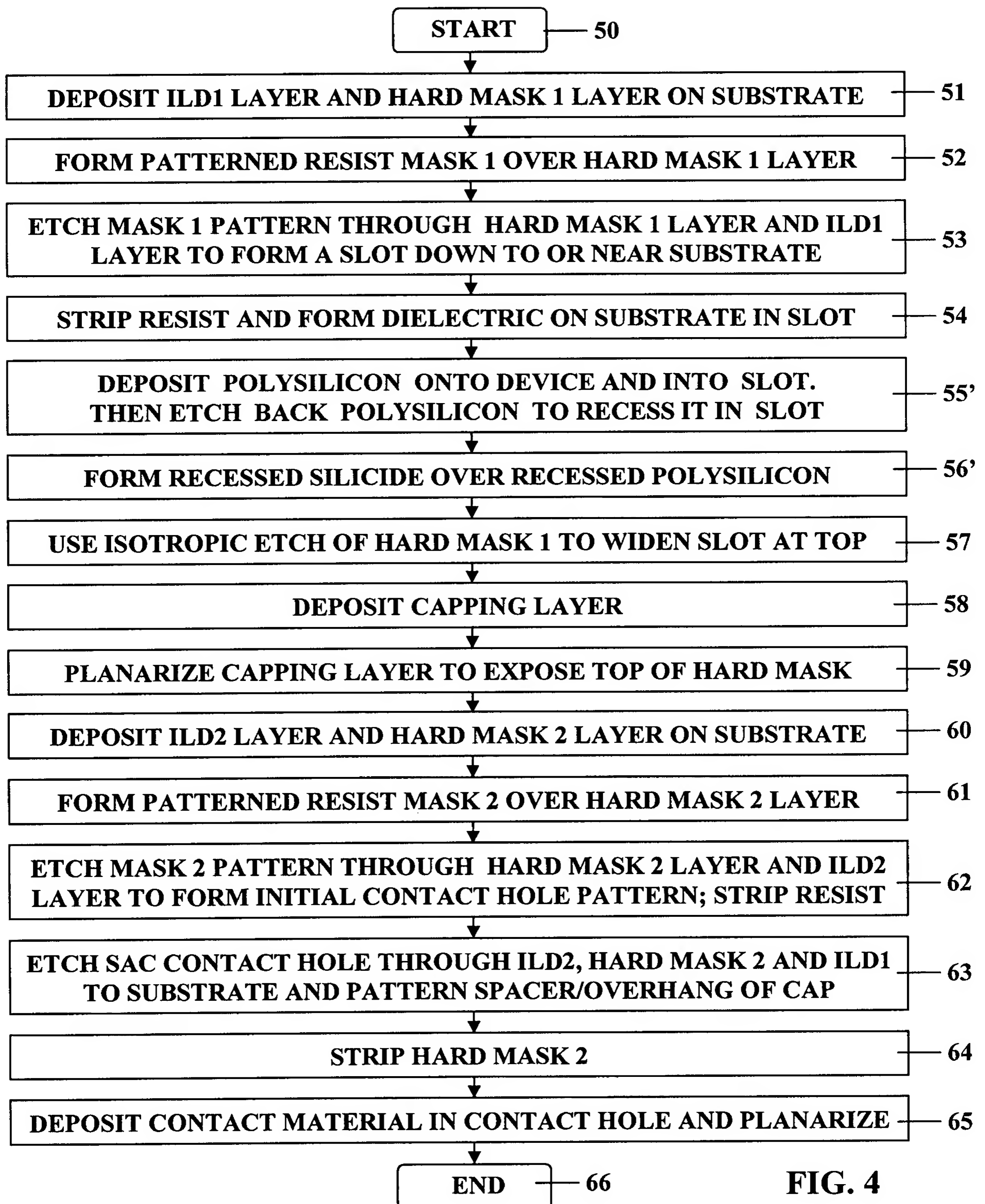


FIG. 4

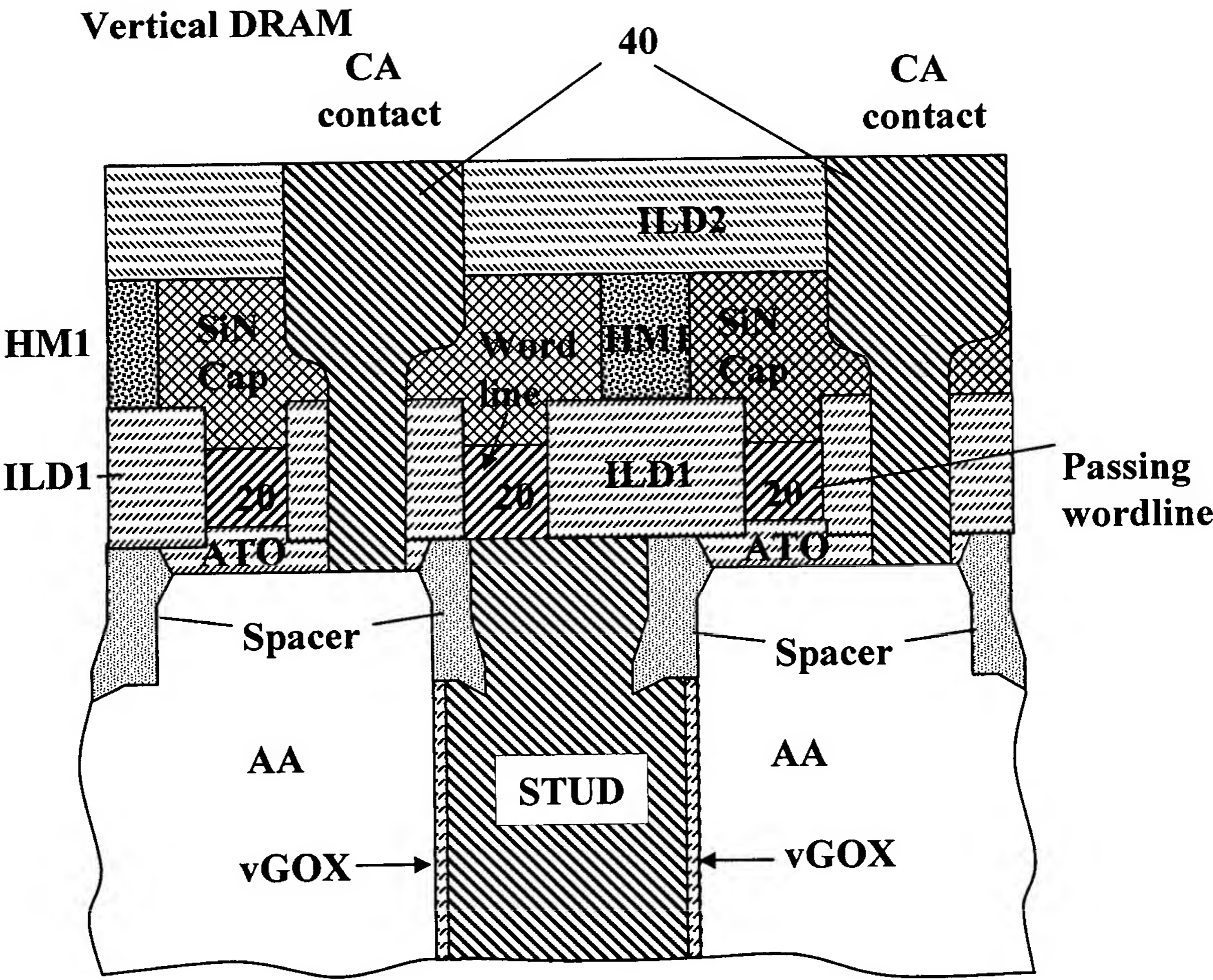


FIG. 5

Planar DRAM

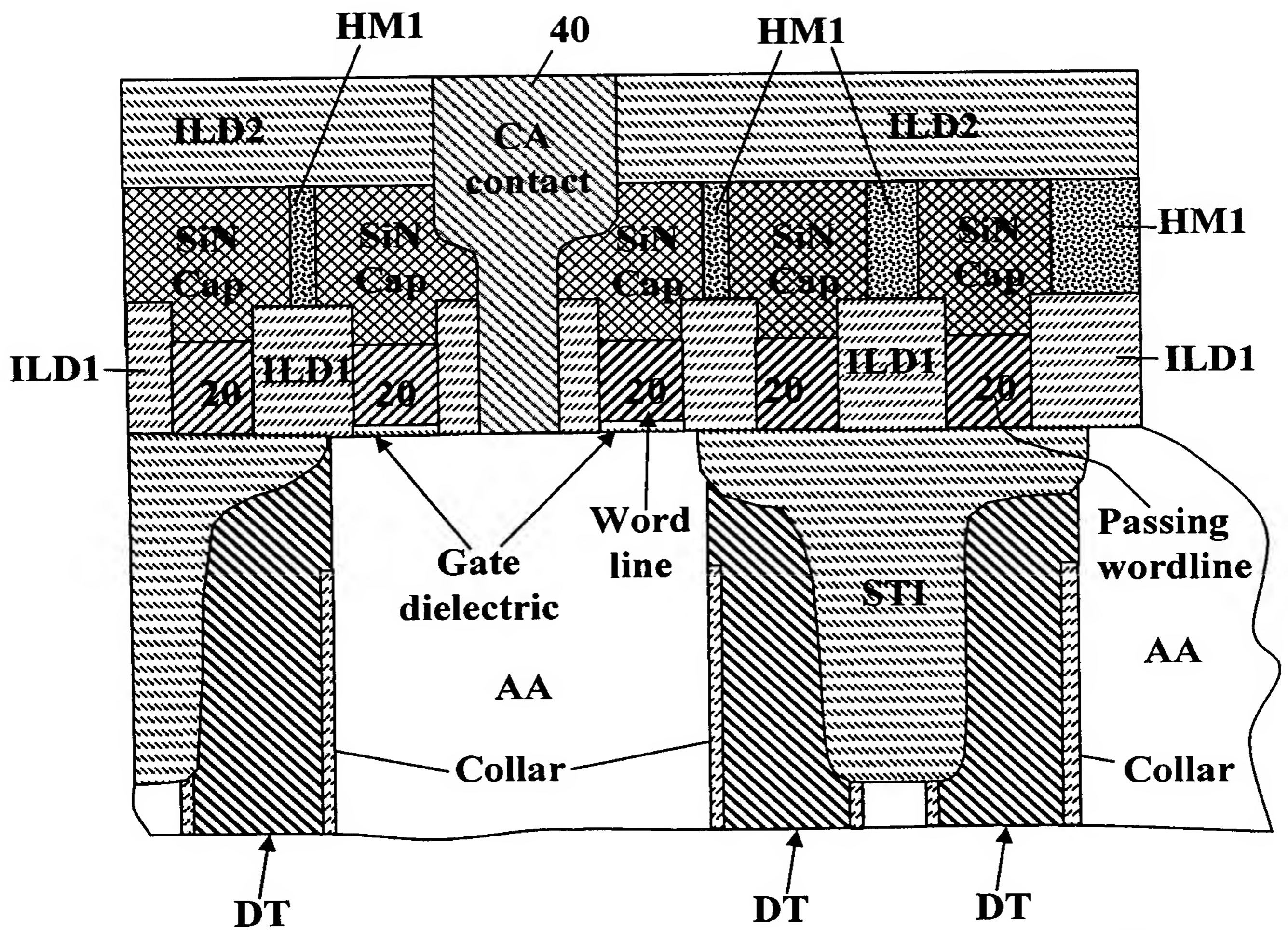


FIG. 6

Stack DRAM

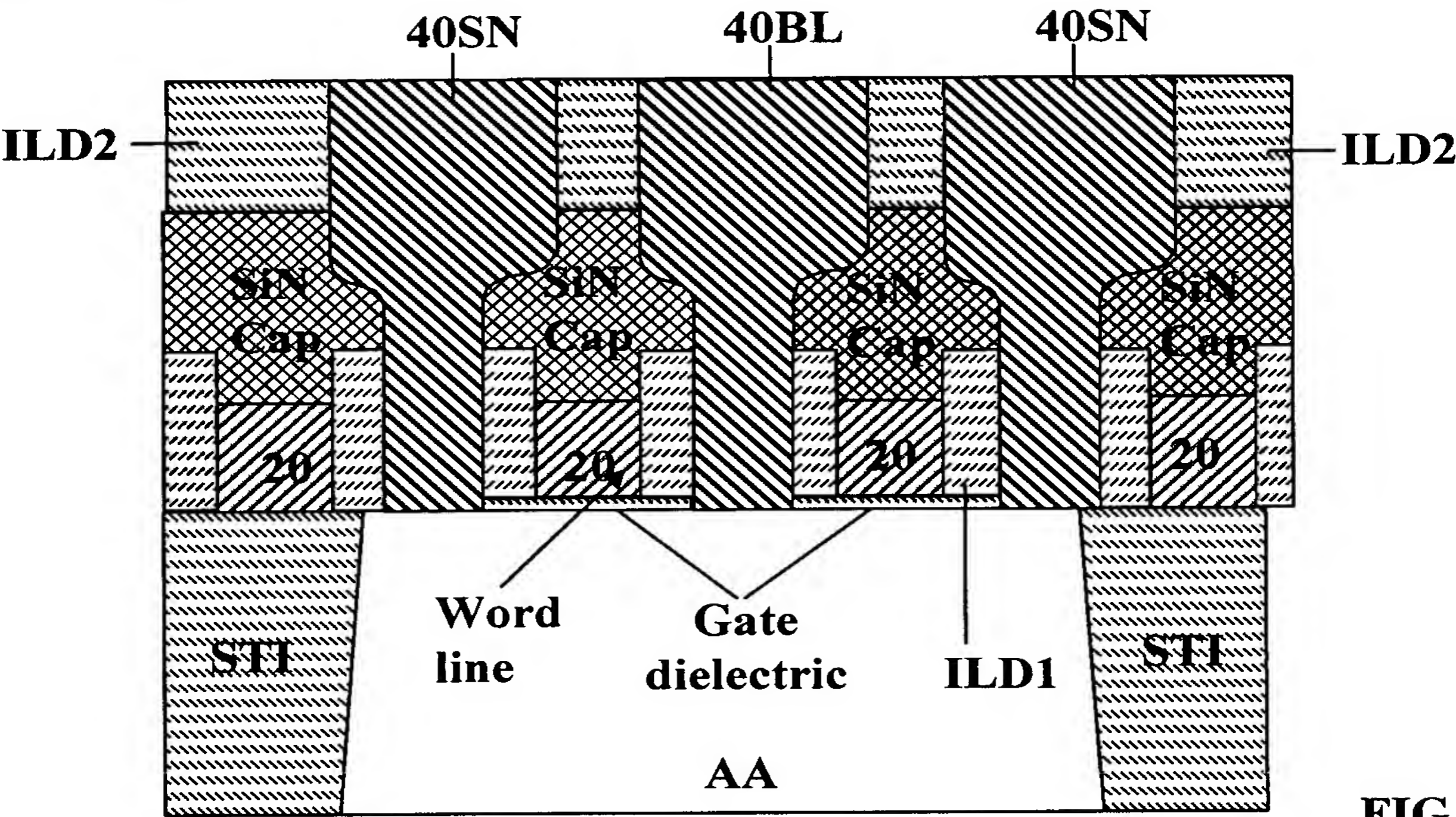


FIG. 7

Metal Gate or SRAM

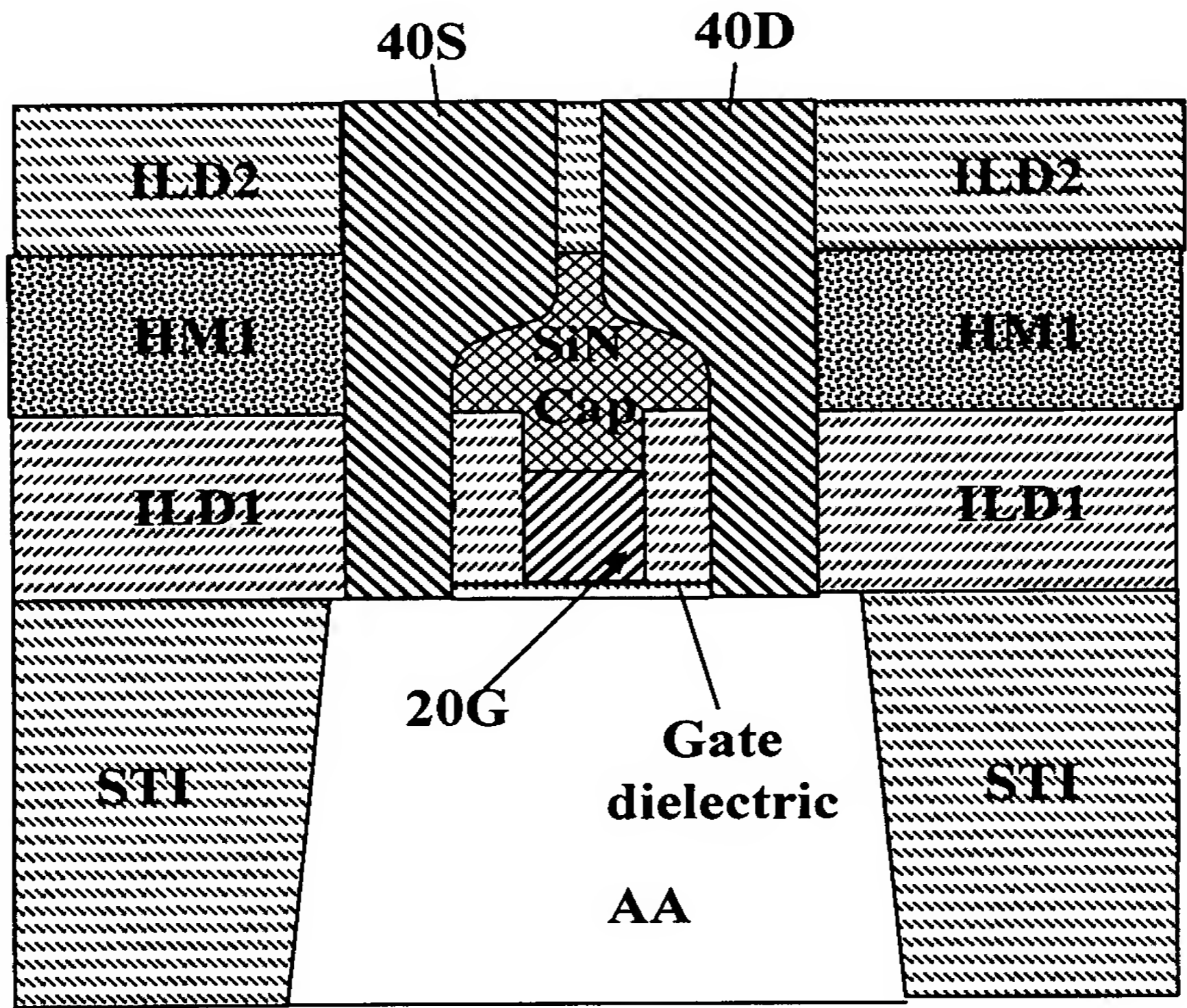
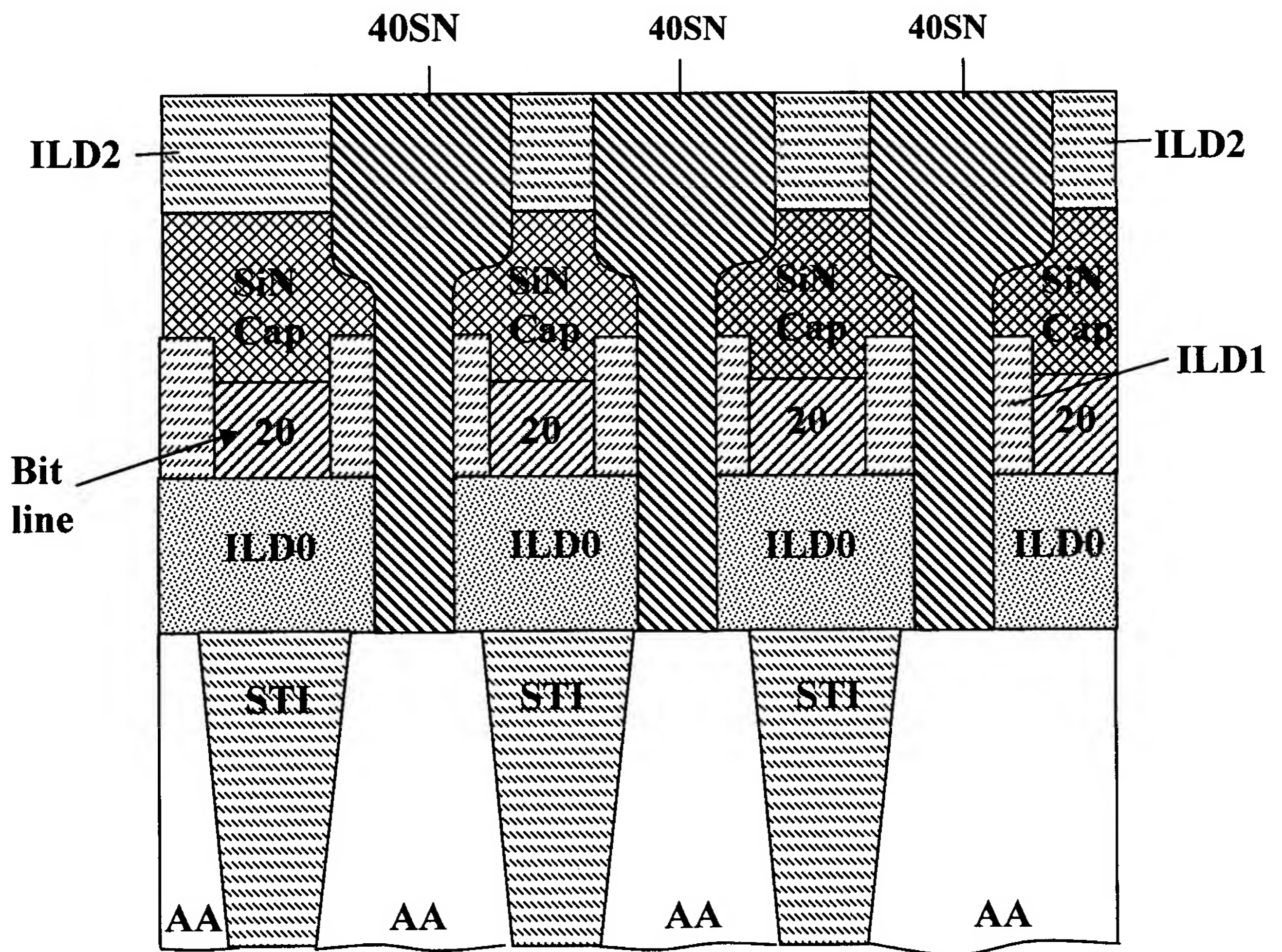
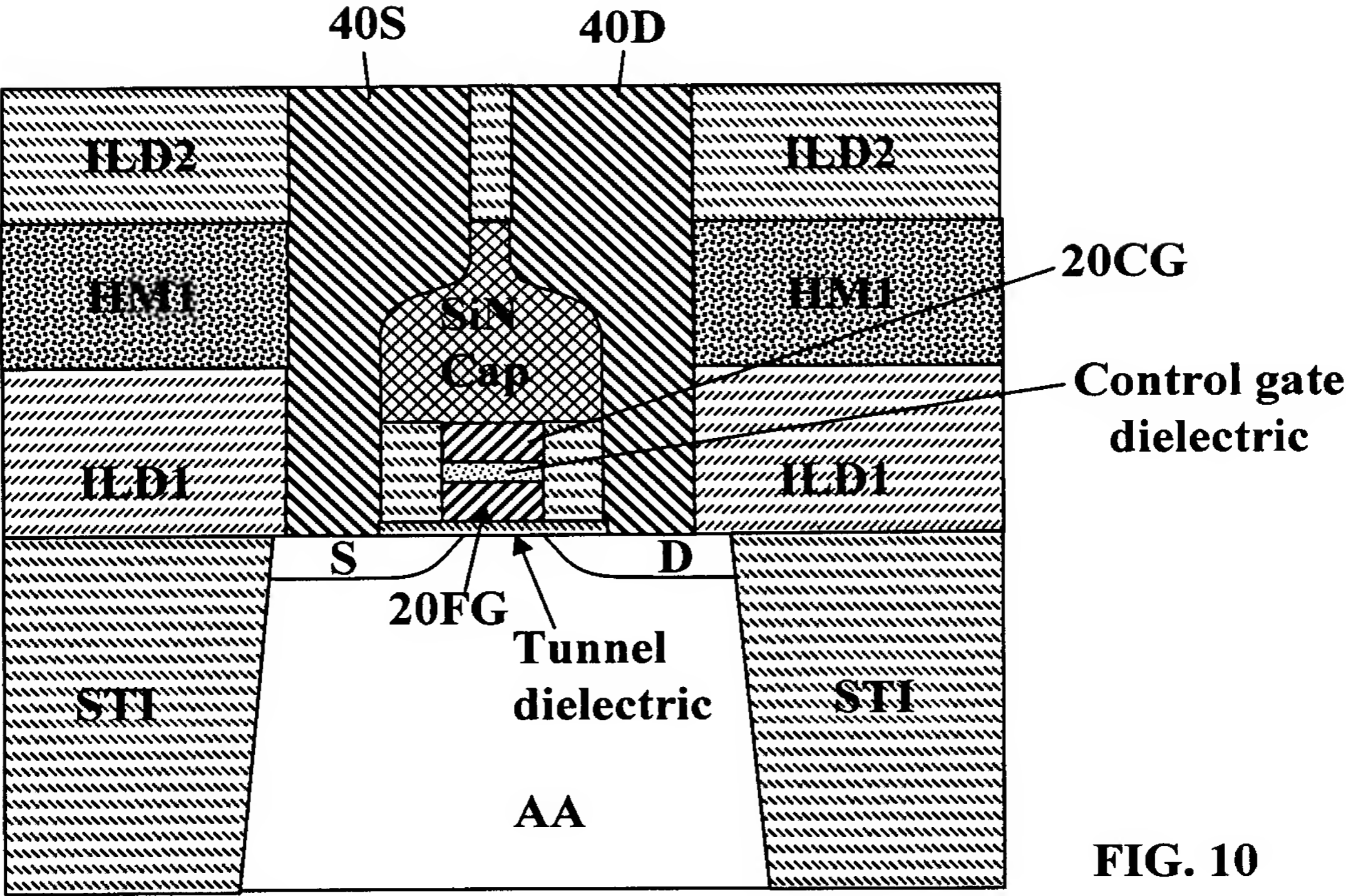


FIG. 8

Capacitor contact over bit line for stack DRAM

**FIG. 9**



High Density Interconnect Line for BEOL

